FRIENDS DEVICES AND THEIR COORDINATION

A thesis submitted
in partial fulfillment of the requirements
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Master of Technology

by

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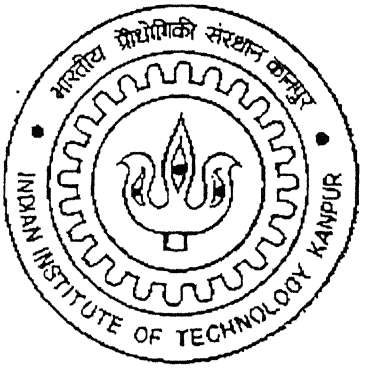

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CERTIFICATE

This is certified that the work contained in this thesis entitled "**FRIENDS Devices and Their Coordination**", by **Ramjee Lal Meena,** has been carried out under our supervision and this work has not been submitted elsewhere for a degree.

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Dedicated to

my parents

Sundar Lal and Tulsi

&

brothers

Bhajan and Bhagwan

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Ramjee Lal Meena

Abstract

Power Quality is the major concern in the present electric power scenario. Dispersed generators are connected to power grid through power electronics based converters. Therefore their protection attains great significance. The FRIENDS (Flexible, Reliable and Intelligent Electrical eNergy Delivery System) is a new concept about the future of the electric power delivery system. To operate the FRIENDS efficiently, power electronics technologies play important roles. Topologies of Static Current Limiter, Static Circuit Breaker and Static Transfer Switch are presented and function of each component is discussed. The working of individual FRIENDS devices is performed with the help of PSCAD/EMTDC software package. Static protective devices are simulated for a radial distribution system. The coordination issues of FRIENDS devices are discussed with their possible solution. For a generic test system the proposed coordination is simulated. The STS is simulated for the single-phase and three-phase R-L passive and regenerative sensitive loads. The results are compared for the SCR and GTO based topologies.

Keywords

Power Quality, Flexible, Reliable and Intelligent Electrical eNergy Delivery System (FRIENDS), Static Switch, Static Current Limiter (SCL), Static Circuit Breaker (SCB), Static Transfer Switch (STS), PSCAD/EMTDC Simulation.

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CHAPTER 1

Introduction

Highly reliable electrical power supplies are needed in modern society where so many microelectronic machines are utilized. For a microelectronic machine, not only a power failure, but also a short-term (few cycles) voltage decrease or increase may cause serious problems. Personal computers may loose important data in a momentary voltage disturbance. Permanent availability of power supply is a vital requirement for a great number of industrial processes. The interruption of critical process due to power outages, voltage sags or interruptions can result in loss of productivity, damaged equipment and products, delay in delivery, costs for cleaning and restart and in worst case injury to people and pollution of the environment. Thus power quality is a very important issue for utilities and industrial market. Continuity in power supply is necessary for a great number of processes and for steady industrial growth.

In a developing country like India dispersed generation will provide power to rural areas through wind, photovoltaic generators, micro turbines, mini hydel plants and biomass etc. Dispersed generators are connected to power grid through power electronics based converters. Therefore their protection attains great significance. Their emergence with the main power grid effects the power quality in a large scale. Thus, the future electrical delivery system must be shaped up such that it is able to correspond to various requirements of electrical power customers. For this the power

supply must utilize several new equipment and technologies that are under development currently.

Problem of poor power quality can be solved by power electronics based FRIENDS devices. The word FRIENDS stands for Flexible Reliable and Intelligent Electrical eNergy Delivery Systems. With FRIENDS, the power system can be operated without interrupting the power supply by flexibly changing the distribution systems configurations after the occurrence of a fault.

1.1 Power Quality

Power quality is simply the interaction of electrical power with electrical equipment. If electrical equipment operates correctly and reliably without being damaged or stressed, we would say that the electrical power is of good quality. On the other hand, if the electrical equipment malfunctions, is unreliable, or is damaged during normal usage, we would suspect that the power quality is poor. As a general statement, any deviation from normal of a voltage source (either DC or AC) can be classified as a power quality issue. For AC transmission and distribution system, power quality broadly refers to maintaining a near sinusoidal bus voltage at rated magnitude and frequency. The power quality of a supply voltage can deteriorate due to very high-speed events such as voltage impulses/transients, high frequency noise, waveshape distortion, voltage swells and sags or due to simple total power loss. Each type of electrical equipment will be affected differently by the power quality issues.

There are two different categories of causes for the deterioration in power quality. The first category contain natural causes such as

- Faults or lightening strikes on transmission lines or distribution feeders.
- Falling of trees or branches on distribution feeders during stormy conditions.

- Equipment failure.

The second category contains man made causes that may be due to load or feeder/ transmission line operation. Some of these are

- Transformer energization, capacitor or feeder switching.
- Power electronic loads such as uninterrupted power supply (UPS), adjustable speed drives (ASD), converters etc.
- Arc furnaces and induction heating systems.
- Switching on or off large loads

1.1.1 Power Quality Terms and Definitions

The power quality standards vary amongst countries. However, poor power quality affects almost all consumers. The important terms used with power quality are discussed here.

- Transient.
- Short duration voltage variations.
- Long duration voltage variation.
- Voltage imbalance.
- Waveform distortions.
- Voltage fluctuations.
- Power frequency variation.

Transient is high amplitude, short duration impulse superimposed on the normal voltage or current. Transient can be classified in to two categories –*impulsive transients* and *oscillatory transients*. An impulsive transient is a sudden, non-power frequency change in voltage, current etc. that is unipolar in nature. Impulsive transients

have a very fast rise time and also a very fast decay time. Lightening strikes mainly cause these transients.

An oscillatory transient is usually bipolar in nature. It has one or more sinusoidal components that get multiplied by a decaying term. Oscillatory transients are classified in accordance to their frequency. An oscillatory transient with a primary frequency greater than 500 kHz is considered *high frequency transients*. A transient within the frequency range of 5 kHz to 500 kHz is considered a *medium frequency transient* and anything below 5 kHz is termed as *low frequency transient*. Typical causes of oscillatory transients are capacitor or transformer energization and converter switching.

Short Duration Voltage Variations are defined as variations in supply voltage for durations not exceeding one minute. These are caused by faults, energization of large loads that require large inrush currents and intermittent loose connection in the power wiring. Short duration variations are further classified as *voltage sags, voltage swells* and *interruptions*. Voltage sag is a fundamental frequency decrease in the supply voltage for duration of 5 cycles to one minute. System faults and energization of heavy loads are causes of voltage sag.

Voltage swells are defined as the increase of fundamental frequency voltage for a short duration. Voltage swells are not common as voltage sags. The main reason for their occurrence is the temporary rise in the voltage of unfaulted phase during a single-line-to-ground fault. The severity of the swell that will be experienced by a load depends on its proximity to the fault location, system impedance and grounding.

An interruption occurs when the supply voltage (or load current) decreases to less than 0.1 per unit for a period of time not exceeding one minute. It is caused by

system faults, equipment failure and control malfunction. The time duration of such an interruption is dependent up on the operating time of the protective device.

Long Duration Variations are defined as the rms variations in the supply voltage at fundamental frequency from its nominal value, for periods exceeding one minute. These variations are classified into *overvoltages, undervoltages* and *sustained interruptions*. An overvoltage (or undervoltage) is a 10% or more increase (or decrease) in rms voltage for more than 1 minute. In a poor voltage regulated system the switching off of a large load or the energization of large capacitor bank may result in an overvoltage. An undervoltage is the result of event, which is a reverse of the event that causes overvoltage.

The term *brownout* is often used to describe sustained periods of undervoltage due to specific utility strategy to reduce power demand. When the supply voltage is zero for a period of time in excess of 1 minute, the long duration voltage variation is called *sustained interruption*. Human intervention is required during sustained interruption for repair and restoration.

Voltage Imbalance is the condition in which the voltages of the three phases of the supply are not equal in magnitude. Furthermore, they may not even be equal displaced in time. The primary cause of voltage unbalance is the single-phase load in three phase circuits. These are restricted within 5%. Severe imbalance (greater than 5%) can result during single phasing conditions when the protection system opens up one phase of the three-phase supply.

Waveform Distortion is the steady state deviation in the voltage or current waveform from an ideal sine wave. These conditions are classified as *dc offset, harmonics* and *notching*. The major causes of dc offsets in power systems are

geomagnetic disturbance and half wave rectification. This forces the transformer core into saturation that destroys the performance of the transformer.

Power electronic loads like UPS, adjustable speed drives etc usually cause harmonics in power system. A measure of harmonic content in a signal is the *total harmonic distortion (THD)*. The percentage THD in a voltage is given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \times 100 \qquad (1.1)$$

where V_n denotes the magnitude of the n^{th} harmonic voltage and V_1 is the magnitude of the fundamental voltage. Similar expression can also be written for current harmonics. Usually for good power quality it is recommended that the THD be less than 3%.

Notching is a periodic voltage distortion due to operation of power electronic converters when current commutates from one phase to other. During this period there is a momentary short circuit between the two phases that distorts voltages. The maximum voltage during notches depends on the system impedance. The frequency components that are associated with notches are usually very high.

Voltage Fluctuations are random variations in supply voltage of the system. A very rapid change in the supply voltage is called *voltage flicker*. This is caused by rapid variations in current magnitude of loads such as arc furnaces. In an arc furnace, a large inrush current flows when the arc strikes first. This causes a dip in the voltage of the bus to which the furnace is connected. Therefore other customers that are supplied by the same feeder face regular severe voltage drops unless the supply bus is very stiff.

Power Frequency Variations are usually caused by rapid changes in the load connected to the system. It is desirable that the supply frequency does not deviate too much from the nominal frequency of 50Hz or 60 Hz. The maximum tolerable variation in supply frequency is often limited within ± 0.5 Hz.

1.1.2 Power Acceptability Curves

These curves quantify the acceptability of power supply in presence of bus voltage disturbance. These plot duration versus magnitude of voltage disturbance [1]. One of these curves was originally developed by Computer Business Equipment Manufacturers Association (CBEMA) to set limits to the withstanding capabilities of computers in terms of magnitude and duration of the voltage disturbance. In the CBEMA curve shown in Fig.1.1 there are two traces – one for over voltage and the other for undervoltage. These show percent bus voltage deviation from the rated

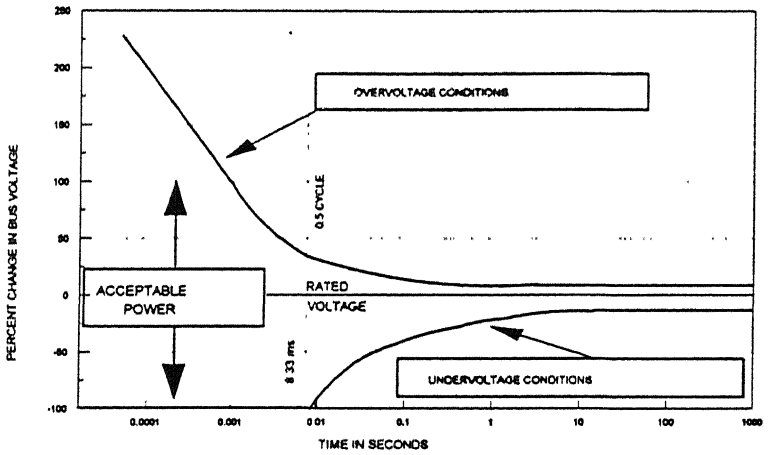

Fig 1.1 The CBEMA curve

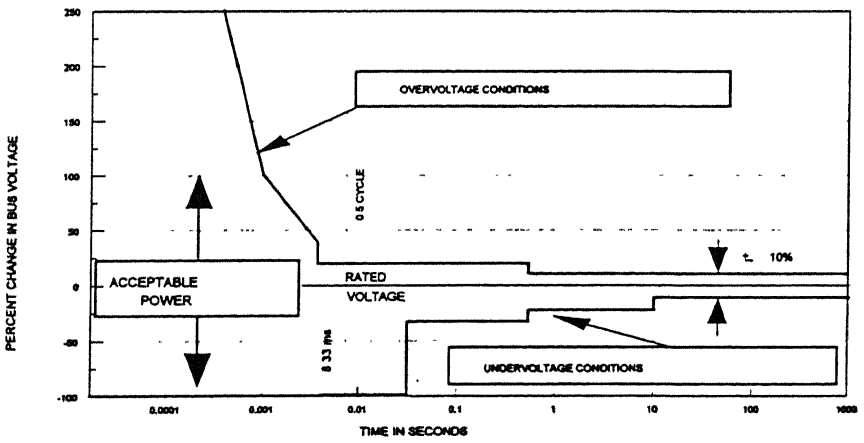

Fig 1.2 The ITIC curve

voltage against time. The region below the upper trace and above the lower trace is the acceptable range. This region defines the tolerance level.

The Information Technology Industry Council (ITIC) redesigned the CBEMA curve in the later half of the 1990. ITIC curve is shown in Fig. 1.2, which describes the acceptable range in steps, rather than smooth curves used in CBEMA.

1.2 FRIENDS

As the worldwide deregulation in the electric power industry progresses, the basic structure of the power systems will change drastically. For example, it is expected that small-scale dispersed type generation facilities such as photovoltaic, fuel cell generation, etc. are installed the power distribution system. Similarly, dispersed type energy storage systems such as secondary battery, electric vehicle, etc. are installed on the demand side as a distributed load. Further, as various customers requirements for power supply such as low pricing of electric power, unbundled power quality services, etc. increase, higher reliability and higher flexibility of the power systems are required. Particularly, the distribution systems, which are closest to the demand side in power systems, are requested to be more user-friendly system than existing distribution systems.

The general concept of FRIENDS is shown in Fig. 1.3 [2-4]. By the above background, many studies on new form of the future power distribution systems (electric energy delivery systems) have started in the world. For example, in the US, studies are being preferred for realizing "Unbundled Power Quality Services". This is a concept whereby electric power of different quality with individual premium is supplied to customers' [5,6]. Currently, a group for researching FRIENDS has been

organized by many researchers from Universities, Electric power companies and Electric power manufacturing companies, etc. in JAPAN.

1.3 Functions of FRIENDS

1.3.1. Unbundled Power Quality Services

The FRIENDS network structure is shown in Fig. 1.4, which can enable various features of power supply to a customer. Some of the features are as follows

(a) Protection against power outages,

(b) Mitigation of voltage sags and swells,

(c) Compensation for transients and harmonics,

(d) Power supply of different reliability,

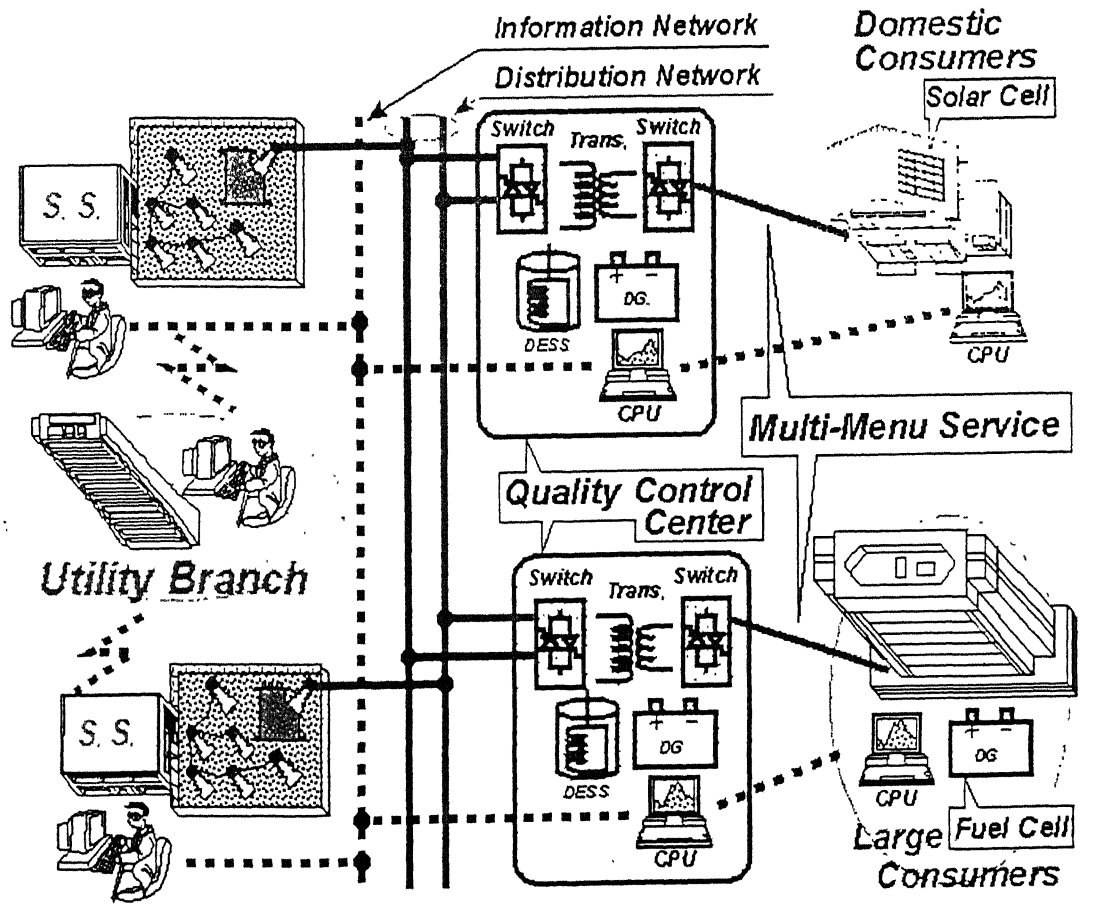

Fig.1.3 General concept of FRIENDS

(e) Interface to dispersed generation systems.

(f) Power supply at DC or other non-standard frequencies.

One of useful function is a multi-menu power supply. The quality control center (QCC) in the FRIENDS produces high quality/expensive and/or ordinary quality/cheap power by utilizing dispersed energy resource and storage. The customers

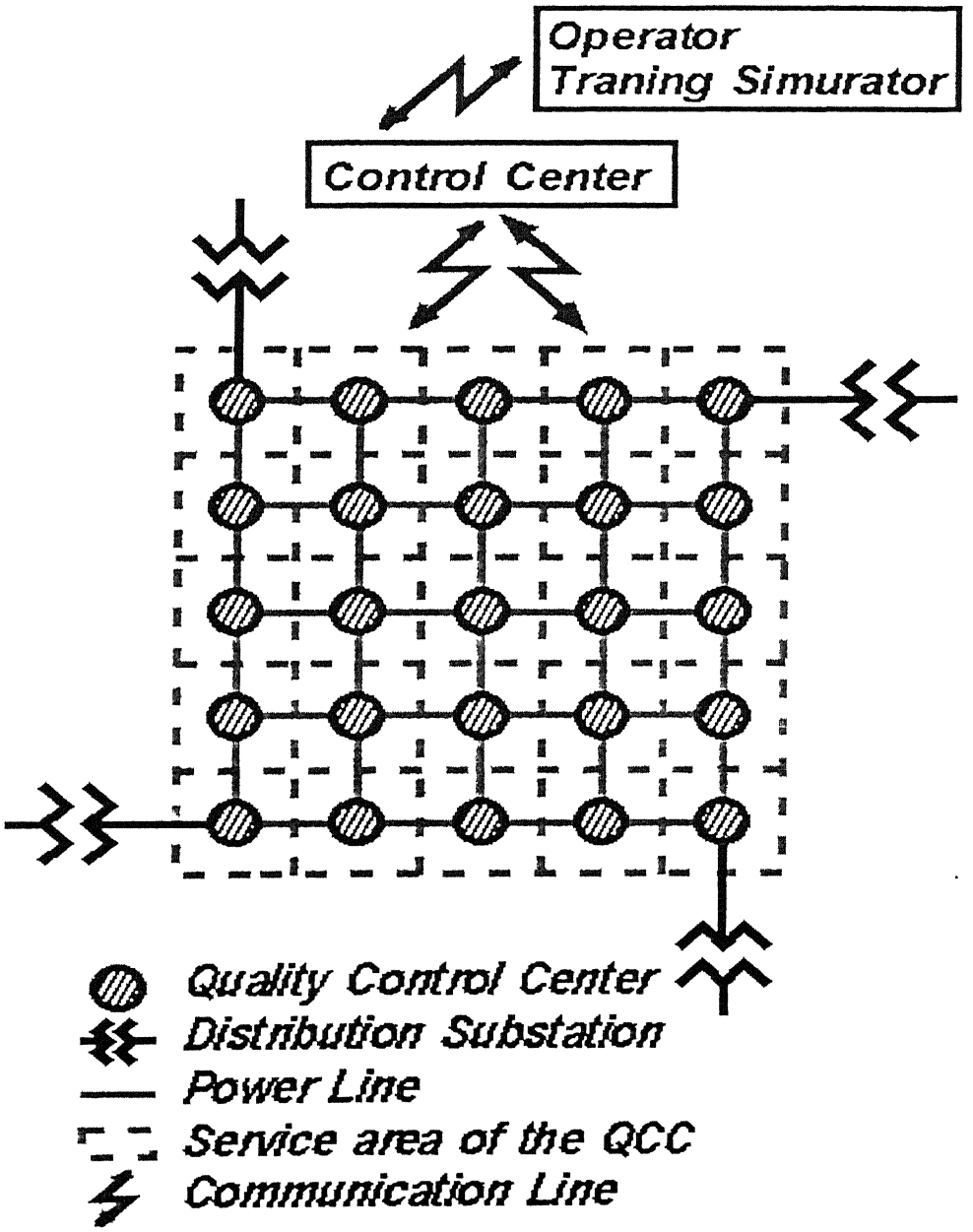

Fig.1.4 FRIENDS network structure

can select the supplier according to the price of the power by automatically selecting the supplier and according the power price. Further, each customer can select the quality of electricity independently through the QCC. More specifically, a multi-menu service for each customer can be provided by bilateral information exchanges.

1.3.2. Flexibility in Configuration of the System

The distribution system configuration should be frequently changed according to the system's states and load patterns in order to avoid power interruptions and to reduce distribution loss. Since the life of mechanical switch depends on the number of switching operations, power electronics switches are preferred for this purpose. One of the most important functions of the power electronics facilities is the fast and low loss switching operation of the system. System configuration of the FRIENDS can be flexibly changed by using power electronics switches in the QCC, so as to achieve loss minimization and fault restoration, etc. As setting of a protective relay must be changed depending on the systems configuration, a computerized protective relaying scheme must be used.

1.3.3. Reliability in Power Supply

The FRIENDS, in principle, never permits power interruption. The dispersed generation facilities such as photovoltaic and fuel cell generation etc. can increase the reliability in power supply. Similarly, dispersed energy storage systems such as secondary battery in the QCC and electric vehicle etc. on demand side can also increase the reliability in power supply That is, these facilities can continue to power supply to customers even in case of fault in high voltage transmission systems. In case of fault at the distribution level, the use of FRIENDS devices isolates the faulted line

by performing a fault state reconfiguration. According to the redundancy of the system, no power interruption occurs in customers.

1.3.4. Intelligent Functions of FRIENDS

The most important role among the computer functions is the high-speed and flexible switching operation of the distribution network, which includes protective relaying functions. This function flexibly controls the static switching facilities (such as GTO thyristor) in the system according to available situation: for example, loss minimization in the normal state, protective relaying scheme in the emergency state and restorative operation in the restoration state. These functions are installed on every computer according to their control level: thus, the functions are achieved on the basis of the dispersed computers. Other important functions are related to the control of dispersed generators and of dispersed energy storage systems, or multi-quality power control and load leveling. These functions are mainly installed on the computers at the QCC.

1.3.5. Load Leveling and Energy Conservation

One of the most important functions in FRIENDS is the load leveling and energy conservation. That is, it is possible to level a load or reduce its peak value effectively by dispersed generation facilities and energy storage systems, which are installed at the quality control center. This function also results in loss reduction in the distribution system. Further, it is expected that dispersed generation facilities (such as photovoltaic and fuel cell generation etc.) and dispersed energy storage systems (such as secondary battery and electric vehicle etc.) be installed on the demand side. In the

FRIENDS, these facilities are controlled and operated efficiently by computers in the quality control center for the load leveling and energy conservation.

1.3.6. Demand Side Prospect

Using the flexible and intelligent features of FRIENDS, customers can have more choices as follows.

(a) Multi-quality power supplies.

(b) Competitive electricity market.

Each customer may choose the service quality. High Quality service will be supplied at appropriate price. A true competitive electricity market can be realized with FRIENDS. Competitive price will be offered for each Independent Power Producer (IPP). Customers may choose several IPPs and utilities to buy from. The efficiency of the system and the consumer surplus will be increased.

1.4. Realization of FRIENDS

Many research results have been published in several areas [2-12], which may be the background technologies of FRIENDS. Important technologies are:

- Power Electronics Facilities
- Information Processing Technologies
- Dispersed Generators and Dispersed Energy Storage
- Deregulation

The realistic diagram is shown in Fig. 1.5.

1.5. FRIENDS Devices

Main FRIENDS devices are:

1. Static Current Limiter
2. Static Circuit Breaker
3. Static Transfer Switch

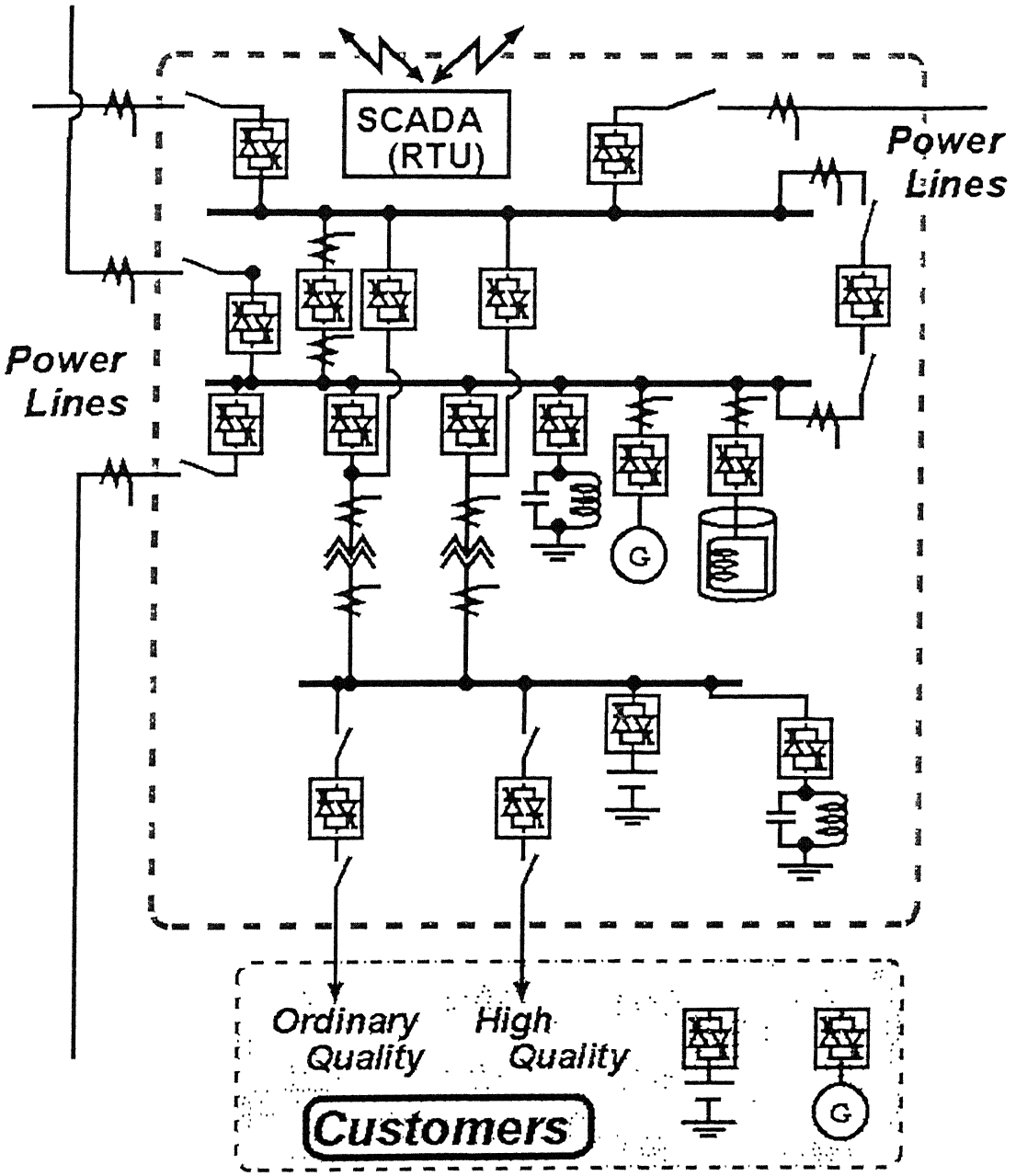

Fig.1.5 Model of quality control center (QCC)

These can be classified according their function. Static Current Limiter (SCL) and Static Circuit Breaker (SCB) are considered as protective devices [13], while Static Transfer Switch (STS) is a control device [14], which is capable to change the configuration of power system network with in short time interval.

Conventionally electromechanical switches are used for breaking and limiting of over-current or short circuit current. This technology to clear a short circuit fault is based on over-current protection system, which typically consists of an over-current relay (OCR), a circuit breaker, current limiting reactor and a section switch with a second auto recloser system. The instantaneous OCR time is 0.2 to 0.5 sec. When a short circuit failure occurs in a distribution line, the feeder circuit breaker, to which the fault line is connected, interrupts the fault current after the relay time. Then after a predetermined short time the breaker is reclosed to restore the power supply. The section switches, which opened because of the loss of line sequentially, close following the circuit breaker reclosing. If the short circuit still exists, a short circuit current flows again when the section switch of the faulty section closes and the feeder breaker interrupts it once again. At this time, the section switch at the faulty section end is opened so that it can not reclose. Then the circuit breaker recloses second time after the relay time and the power is supplied to the sound sections.

Once a fault occurs, three is a short-term power interruption or voltage decrease, which continues for 0.2 or 0.5 sec. This may happen twice as mentioned above. In order to decrease the duration of disturbance, it is effective to have a breaker capable of operating as soon as the fault occurs.

This goal can be achieved by fast operating power semiconductor devices viz. Silicon Controlled Rectifier (SCR), Gate Turn Off thyristor (GTO) etc. The circuit breaker can be replaced by fast static switch, which consists of two anti parallel GTOs

and Over-Current Relay (OCR) is replaced by static trip unit which includes voltage and current sensors, control and firing circuits. Using this new technology the duration of voltage disturbance reduces.

There are two important issues that must be considered before connecting a static current limiting or breaker device in a distribution system. The first and foremost issue is the identification of locations in the system where such devices can be placed. The second issue to be considered is the coordination of the protective devices. Once a limiter or breaker is placed in a system, it must not come in the way of down stream protective devices.

The load transfer switch is usually used for sensitive loads that are connected to two incoming feeders or utilities [14]. At any given time the load is supplied by one of the two feeders. Conventionally mechanical auto transfer equipment is used to switch major industrial and commercial facilities from one feeder to another, a process that typically takes 0.3 second to several seconds.

The speed of transfer does not fulfil the expectations of the bounds suggested by the ITIC curve. The ITIC curve points out that, on average, most sensitive loads can with stand a maximum outage of one half-cycle duration. The Static Transfer Switch (STS) selects, at high speeds between two or more sources of power and provides the best available power to the electrical load downstream and fulfils the requirement of CBEMA curve.

1.6 Objectives of the Thesis

The general aspect of power quality is emphasized Elementary detail of FRIENDS is discussed. The main functions of FRIENDS are illustrated in detail. Static current limiting and breaking devices protects the distribution system fast and

efficiently. STS transfers supply between two or more ac sources when applied at critical facilities. Thus the FRIENDS devices improve the flexibility, reliability and perform intelligently.

The objectives of the thesis are to simulate FRIENDS devices in PSCAD/EMTDC software package and study their coordination aspects to determine their placement location in a generic distribution system. Also operating parameters are calculated for providing a fast and reliable protection.

The simulation for static circuit breaker and static current limiter is presented in Chapter 2 for various operating and fault conditions. The results for different component value are compared. Static transfer switch based on SCRs and GTOs are also simulated in Chapter 2. Their performance and suitability is analyzed. The coordination problem is studied in Chapter 3 for a generic distribution system. The results for different fault conditions are discussed. The three-phase applications of STS to IEEE benchmark system [15] for passive and active loads are simulated in Chapter 4 and the results are analyzed. The conclusion is given in Chapter 5 where the scopes for future work are also suggested

CHAPTER 2

Simulation of FRIENDS Protection Devices

In efficient operation of the FRIENDS static devices, using power electronics technologies play important roles. These static protection and control devices are discussed in this chapter. Power electronics based *static switch* is the building block for all FRIENDS devices. GTOs are used for Static Current Limiter (SCL) and Static Circuit Breaker (SCB) where instantaneous current has to be interrupted. SCRs are used for Static Transfer Switch (STS) where transfer of power from one source to another is performed. GTOs can be used for STS instead of SCRs to make them faster. The following sections describe the operation of SCL, SCB and STS. The operation has been verified by simulation using PSCAD/EMTDC.

2.1 Static Switch

The static switch is the basic building block of all protecting and control devices. Topology of static switch is shown in Fig. 2.1. This is the combination of two anti-parallel thyristors. The function of static switch is explained in Fig. 2.2. Assume that an alternating current flows from the left to the right of the static switch. The positive half cycle of switch current I_{sw} is passed by the thyristor T_1 that is in forward biased condition. Similarly the negative half cycle current is passed by the other thyristor T_2. Thus each thyristor conducts for half cycle and remains in the off state for another half cycle. Blocking the firing signal can interrupt the current flowing through static switch. The current will then be interrupted at its next zero crossing.

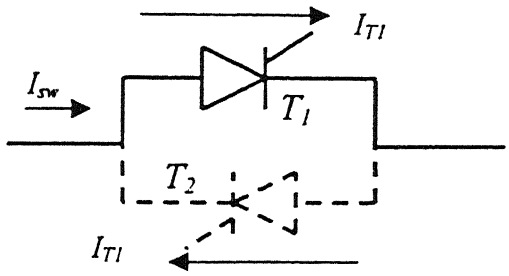

Fig. 2.1 A static switch

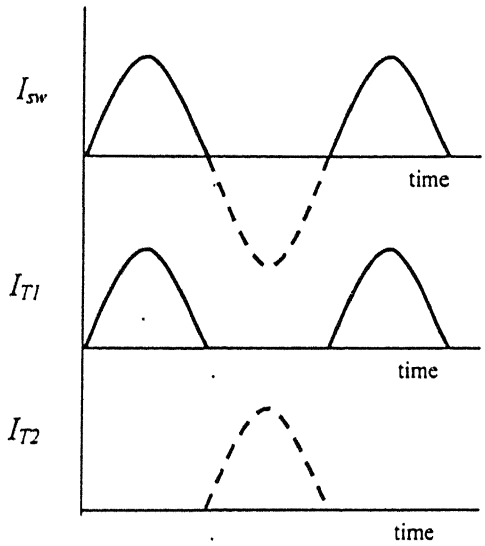

Fig. 2.2 Current waveforms through static switch

When thyristors are replaced by gate turn off thyristors (GTOs), the operation will be faster because current can be forced to zero at any instant, therefore eliminating the need to wait till the next zero crossing. This characteristic is mandatory for current limiting and breaking devices, because the peak of first half cycle of fault current may damage the static switch as well as other power system apparatus. For load transferring, thyristors are sufficient but GTOs may transfer faster than thyristors. Simulation result given later shows that the GTOs will speed up the transfer by at least 2 ms which will improve the power quality. However till now the high cost prevents their use in the commercial transferring devices.

2.2 Static Current Limiter (SCL)

Topology of SCL is shown in Fig. 2.3. The GTO based static switch and let-through reactor are connected in parallel. A snubber circuit (not shown in figure) is used to protect the GTO from large *dv/dt*. The ZnO arrester limits the peak voltage appearing across the switch during turn-off. Under normal load conditions, the GTOs are gated continuously and maintained in full conduction thus passing the feeder current I_f. When a fault occurs on the load side of SCL, a control circuit, activated by the instantaneous magnitude of the fault current, initiates a turn-off for the GTOs. The GTOs respond within a few microseconds of the control signal and are capable of turning off current considerably higher in magnitude than the maximum continuous current. Immediately after the GTO turns off, the current will be diverted in to current limiting reactor and arrester. Thus the fault current is quickly limited before it reaches a destructive level.

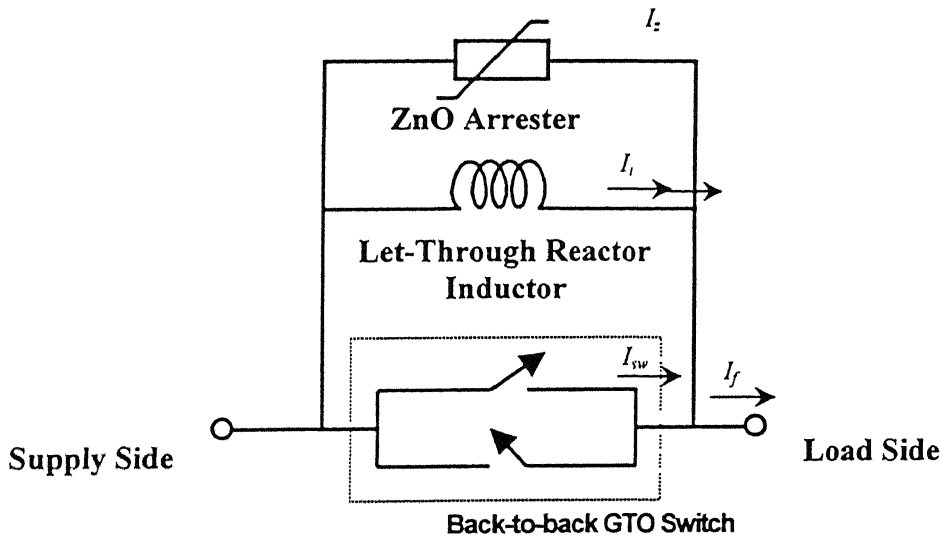

Fig. 2.3 GTO-based SCL topology

2.3 Static Circuit Breaker (SCB)

The schematic diagram for SCB is shown in Fig. 2.4 .The main components of this device are a high-speed vacuum circuit breaker (VCB) and a GTO based static

switch connected in parallel. The usual load current is carried out by the VCB. In case of system fault, the fault current is commutated to and interrupted by the GTO based static switch by opening the vacuum switch. Therefore the static switch does not require a large cooling system and is compact compared to systems using GTO switch conventionally e.g. SCL.

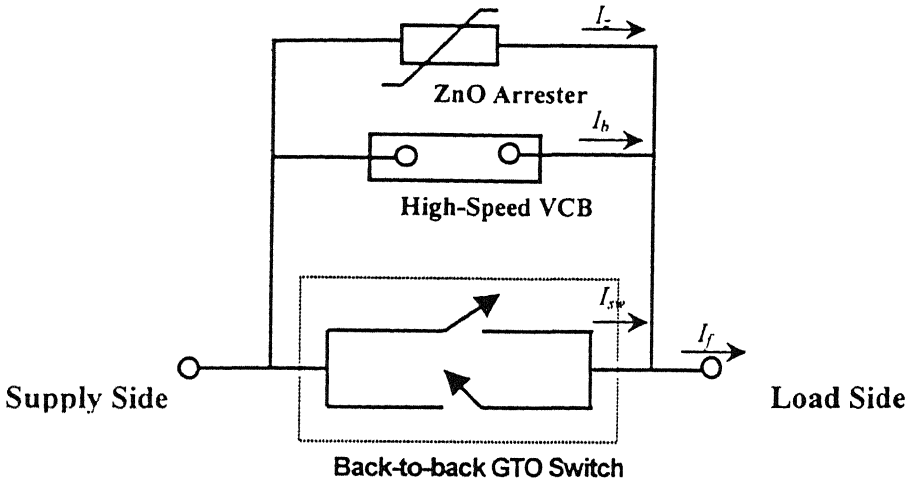

Fig. 2.4 GTO and VCB based SCB topology

2.4 Static Transfer Switch (STS)

The thyristor based STS is illustrated in Fig. 2.5. It is device used to transfer the power from the preferred to the alternative source in the event of a fault. For power quality related problems caused by voltage sags and swells, lightening strikes and other system related disturbances, in many instances, the use of a static transfer switch (STS) can be one of the most effective solutions. The success of the device is mainly due to its low cost and fast response. It used a fast switching strategy, usually referred to as "make before break" switching (MBB).

The name MBB refers to the possibility of firing the thyristors of the static switch that is not conducting (secondary source), thus initiating the transfer, before the current on the corresponding switch in the primary source has become zero. It is

possible to gate the thyristors such that, a current will start flowing in the thyristor that has just been fired in a direction that will force the thyristor that was conducting, to turn off very quickly.

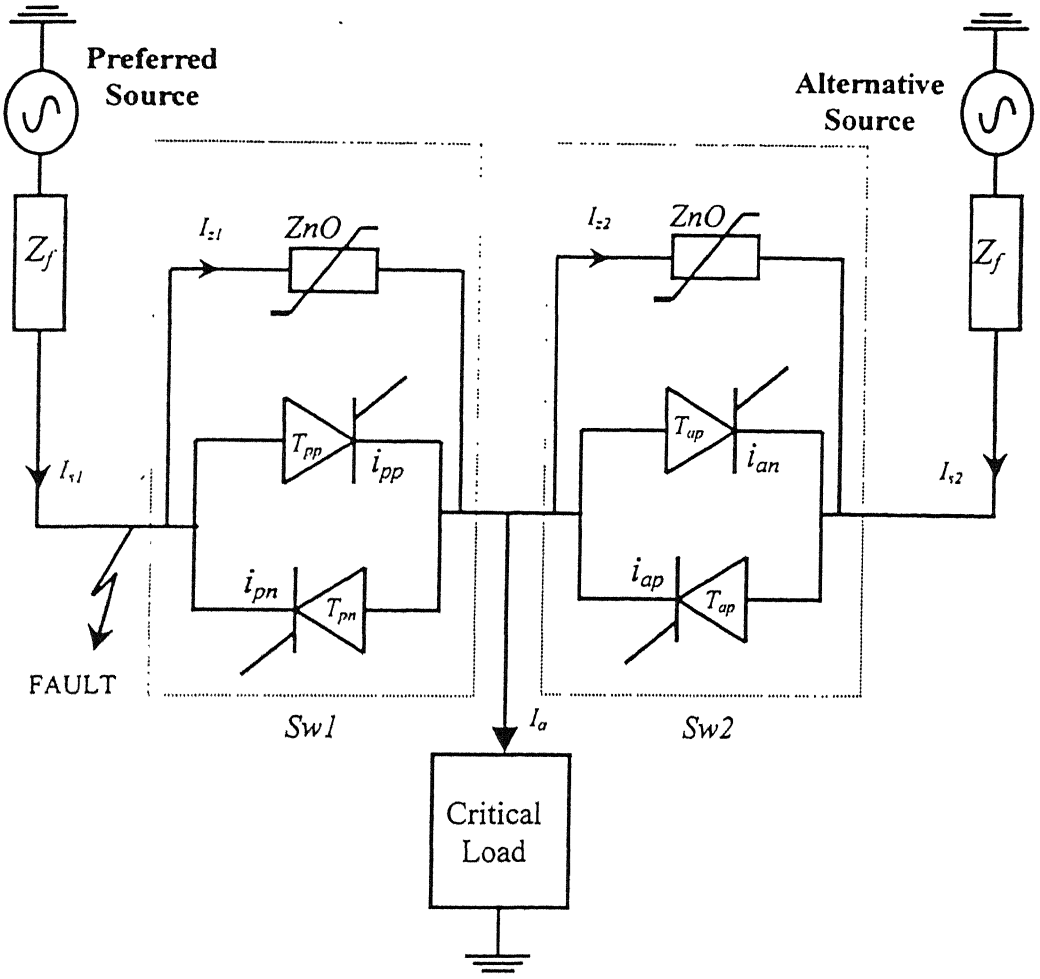

Fig. 2.5 Thyristor based STS topology

The transfer time depends on the type of disturbance and on actual operating conditions of the power system when transfer is initiated. The nature of the transfer however will depend on many factors. Some of these factors are: relative magnitude of the source voltages, phase angle difference between the preferred and alternate sources, feeder impedances, load impedance, fault detection time, whether load is passive or active etc. The nature of the load current during transition will depend on the combination of these parameters. The design of the transfer control must take into

account all these factors for satisfactory operation. Note that in a GTO based STS topology, the thyristors of Fig. 2.5 are replaced by GTOs.

2.5 Simulation Studies

Digital simulations for static protection and control devices are performed using PSCAD/EMTDC software package (version 3.1.7) on a personal computer. For SCL and SCB a simple radial distribution system that is supplying an R-L load as shown in Fig.2.6 is used as a test system. The line to neutral voltage is 6.35 kV (rms) and the system frequency is 50 Hz. The feeder has a resistance of 3.025 Ω and an inductance of 38.5 mH while the load resistance and inductance are given by 60.5 Ω and 770.3 mH respectively. This implies that for a base voltage of 11 kV (L-L) and a base MVA of 1.0, the feeder impedance is 0.025 + j0.1 per unit and the load impedance is 0.5 + j2.0 per unit. The pre fault current in the steady state is 24.25 A (rms), i.e., 0.462 per unit. For a short circuit fault, when only the feeder impedance limits the current, it has the peak of about 1200 A, i.e., more than 20 per unit.

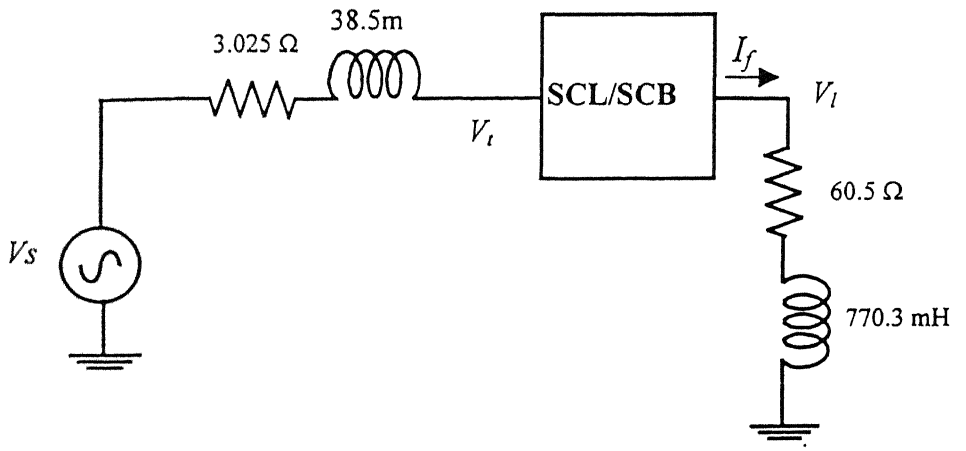

Fig.2.6 Radial distribution protected by SCL

The simulation for STS is done similarly using the topology shown in Fig 2.5. Both Preferred and Alternative sources have line to neutral voltage 6.35 kV (rms) and

the system frequency 50 Hz. Each upper stream feeder has a resistance of 3.025 Ω and an inductance of 38.5 mH The critical load has resistance and inductance 60.5 Ω and 770.3 mH respectively. Thus the value of critical load current is 24.25 A. In this case the short circuit fault is assumed to occur at the input of SW_1 as shown in the above-mentioned figure.

The simulation studies have been carried for protection using the following three devices.

- Case-a: Static Current Limiter (SCL)
- Case-b: Static Circuit Breaker (SCB)
- Case-c: Static Transfer Switch (STS)

In each case the operation of the protective devices has been studied using the per phase equivalent circuit for a short circuit fault at or near the load terminal. Successful operation of the protective devices has been illustrated by waveforms of voltages and currents in the test system.

2.6 Simulation Results and Discussions

2.6.1 Case-a: Static Current Limiter

The SCL (Fig. 2.3) is connected in line to limit the fault current. The value of the let-through inductor is chosen as 500 mH and the clipping voltage level of the ZnO arrester is chosen as 6.9 kV. The system response to a short circuit at the load terminal at time t = 0.21 sec is shown in Fig. 2.7.The load voltage falls to zero immediately and the load current free wheels to zero in local loop. The feeder current magnitude is sensed and the GTO based static switch is commutated as soon as the current reaches 40 Amps (0.76 pu). The current through the let-through inductor can not rise instantaneously. Therefore initially the feeder current passes through the ZnO arrester.

Later the feeder current flows through the let through inductor and the arrester in parallel. As seen in figure the feeder current is has to a peak of about 105 Amp (2 pu). Thus the fault level is reduced from the value of about 20 to 2 pu by the use of SCL. The voltage across the Static Switch is limited to 6.9 kV by the arrester. Again the Fault current is the sum of the current I_1 and I_2. The arrester current dominates this current.

If the arrester voltage level is increased to13.8 kV, the system response is shown in Fig.2.8 For the transition period the snubber circuit, let through inductor and ZnO arrester provide parallel paths to the fault current. Now the let through inductor current is predominantly the fault current. It may be noted that increasing the voltage level reduces the arrester current. This will however increase the voltage across the Static Switch. In Fig. 2.7 it is 9 kV which is the about the peak of the system voltage because the arrester clipping voltage level is higher than the peak of the system voltage

2.6.2 Case-b: Static Circuit Breaker

The SCB is simulated for the same feeder as in case-*a* above Simulated result is shown in Fig 2.9.The fault is created at t = 41 ms. The fault current flowing through Feeder and VCB is sensed and compared with a specific limit that is 2 pu. The GTO based Static Switch is turned on when the feeder current crosses the limit. At the same time a trip signal is given to the VCB and it is assumed to turn off on its own. The turn off time is very small and may be neglected

The GTO based Switch is kept on for a short fixed time interval (1.25 ms) as there is no current limiting inductor in this topology. At the end of this interval the switch is commutated. The total time interval to interrupt the fault current depends upon the time instant when the fault occurs and the value of the current limit. The total

interrupting time for the fault at time t = 41 ms is observed to be 4 ms, which is much smaller than that of the mechanical circuit breaker. In this topology the arrester current is smaller than SCL topology as GTO is used to interrupt the fault current

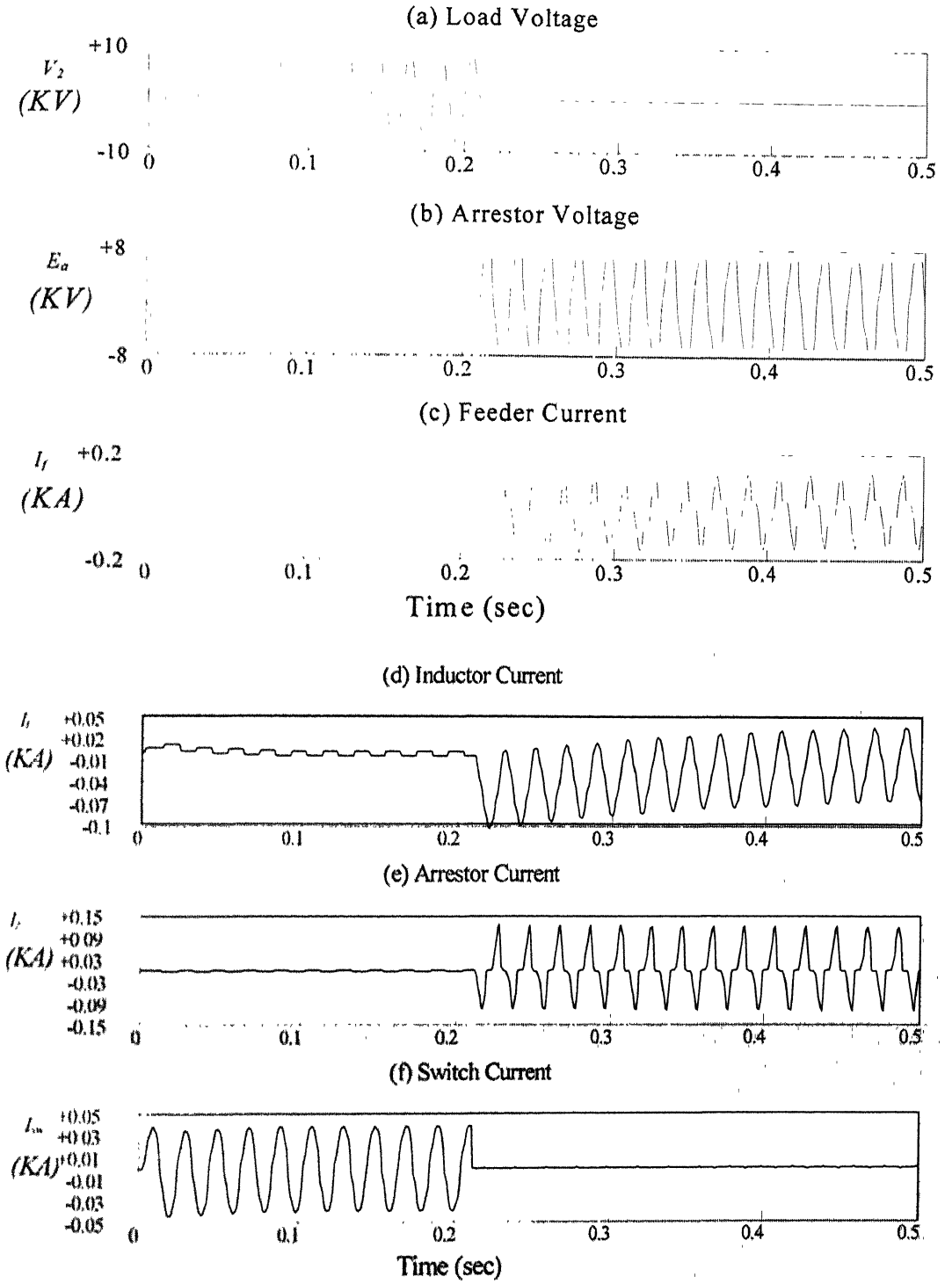

Fig.2.7. SCL protected system response for an arrester clipping voltage level 6.9 kV

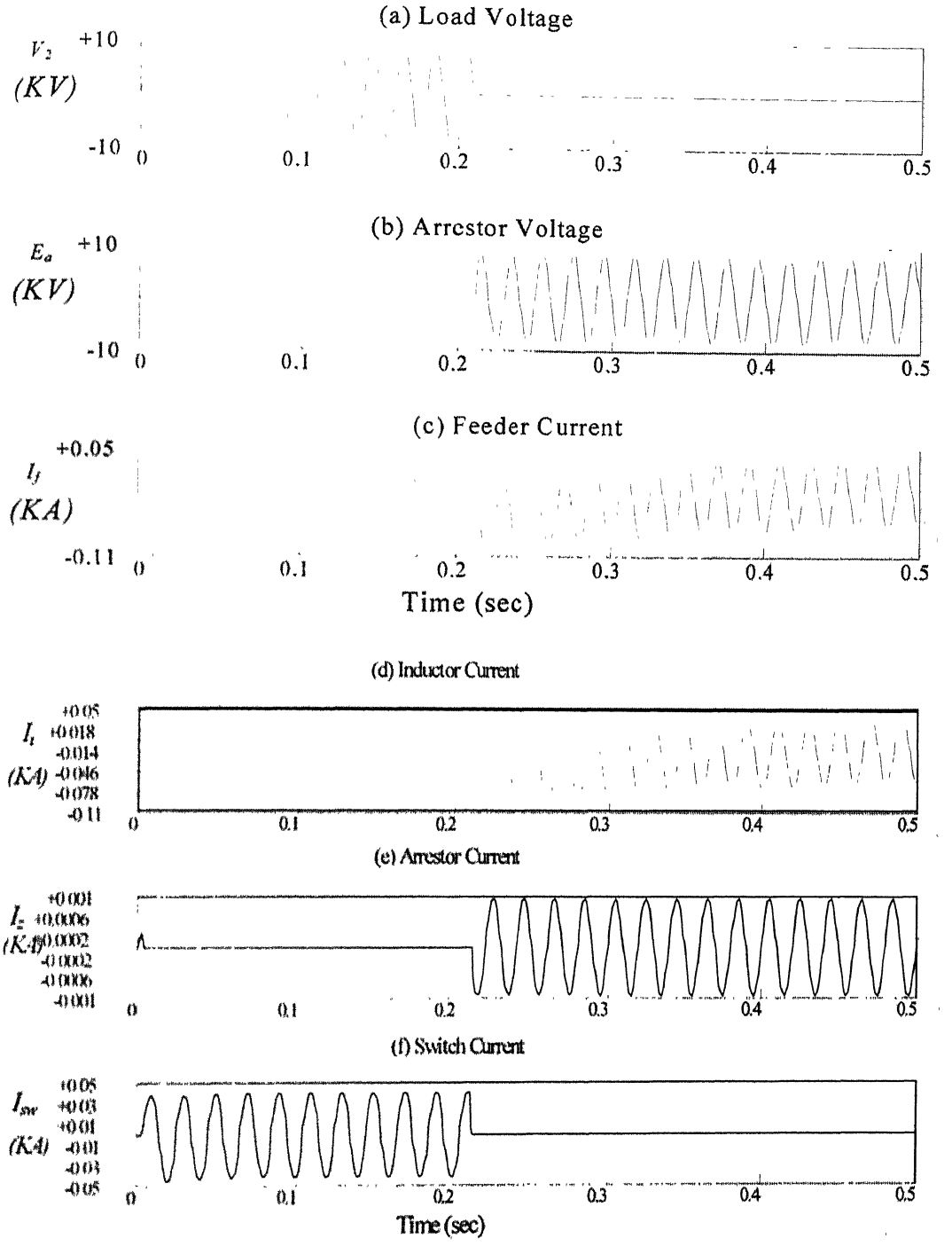

Fig.2.8. SCL protected system response for an arrester clipping voltage level 13.8 kV

2.6.3 Case-c: Static Transfer Switch

The system topology for this case is shown in Fig.2.5 and it is assumed that a fault occurs on the preferred feeder. Simulation result for thyristor based STS switch is

shown in Fig.2.10 with make-before break strategy. The currents through each SCR is also shown in Fig 2.11.The typical transfer time is observed to be 8 ms but this is not a constant for all the conditions. It varies from 7 ms to 12 ms and depends factors like the relative magnitude of source voltages and their phase difference, feeder impedance, load impedance, fault detection time etc.

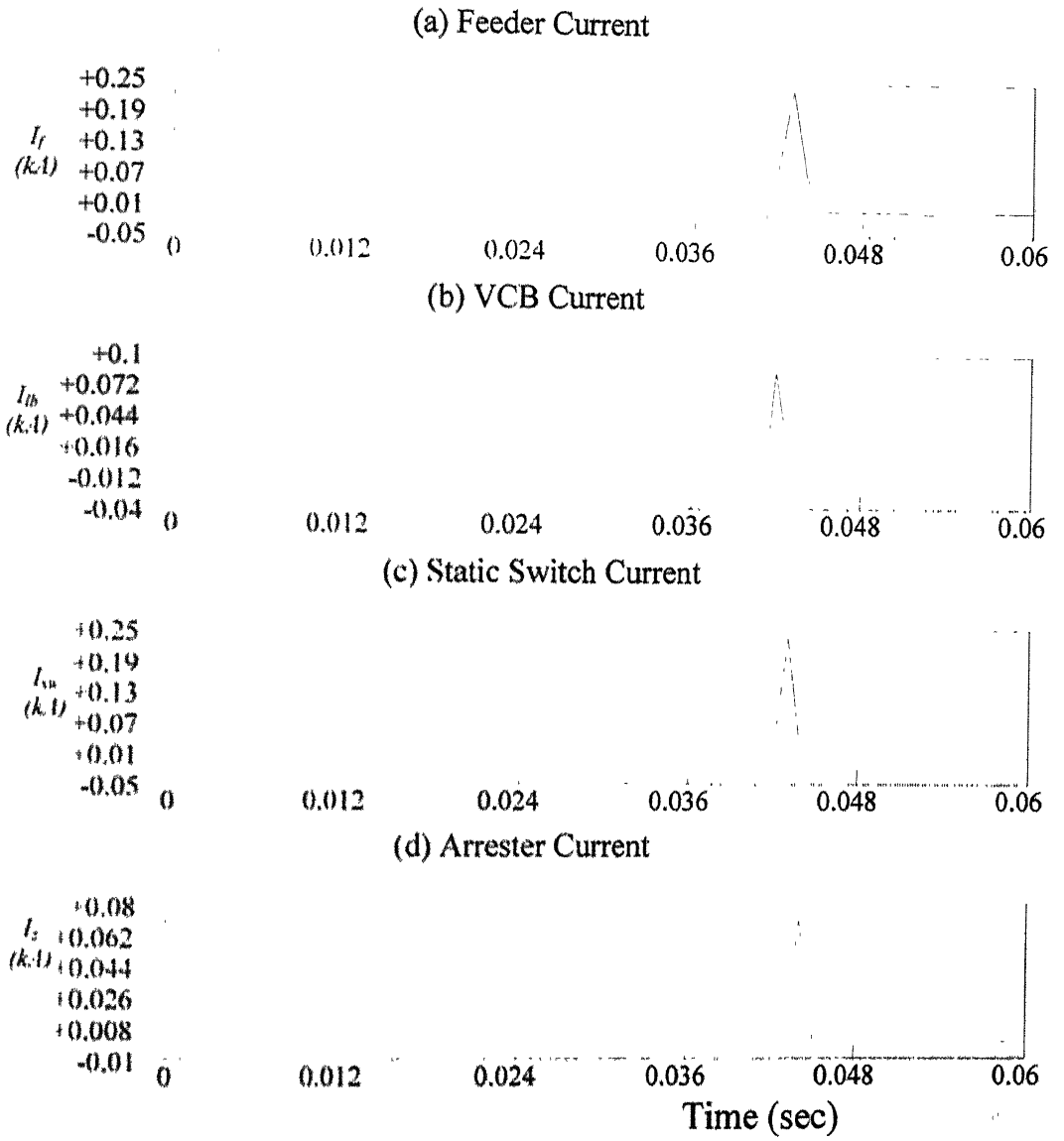

Fig.2.9 System response with SCB

Now consider the case when there is a fault in the preferred feeder. The rms value of the voltage in the preferred feeder is monitored and a fault is detected if this voltage falls below a threshold value. As shown in Fig 2.5, when load current is

passing through thyristor T_{pp} and the control unit detects fault. It will stop firing pulses of static switch S_{w1} and simultaneously issue the triggering pulses to the switch S_{w2}. There may be two possibilities 1) thyristor T_{an} may be in forward biasing 2) thyristor T_{ap} may be in forward bias. These conditions are functions of relative phase difference of source voltages, load power factor, feeder and source impedances and fault instant etc. If first condition take place it will force the T_{pp} to commutate because this will be in reverse biasing. But the second condition will make T_{pp} in forward biasing which lead to transfer the fault current to the alternative source side for a next zero crossing. Similar phenomenon will take place when out going thyristor is T_{pn} only incoming thyristor will interchange their role.

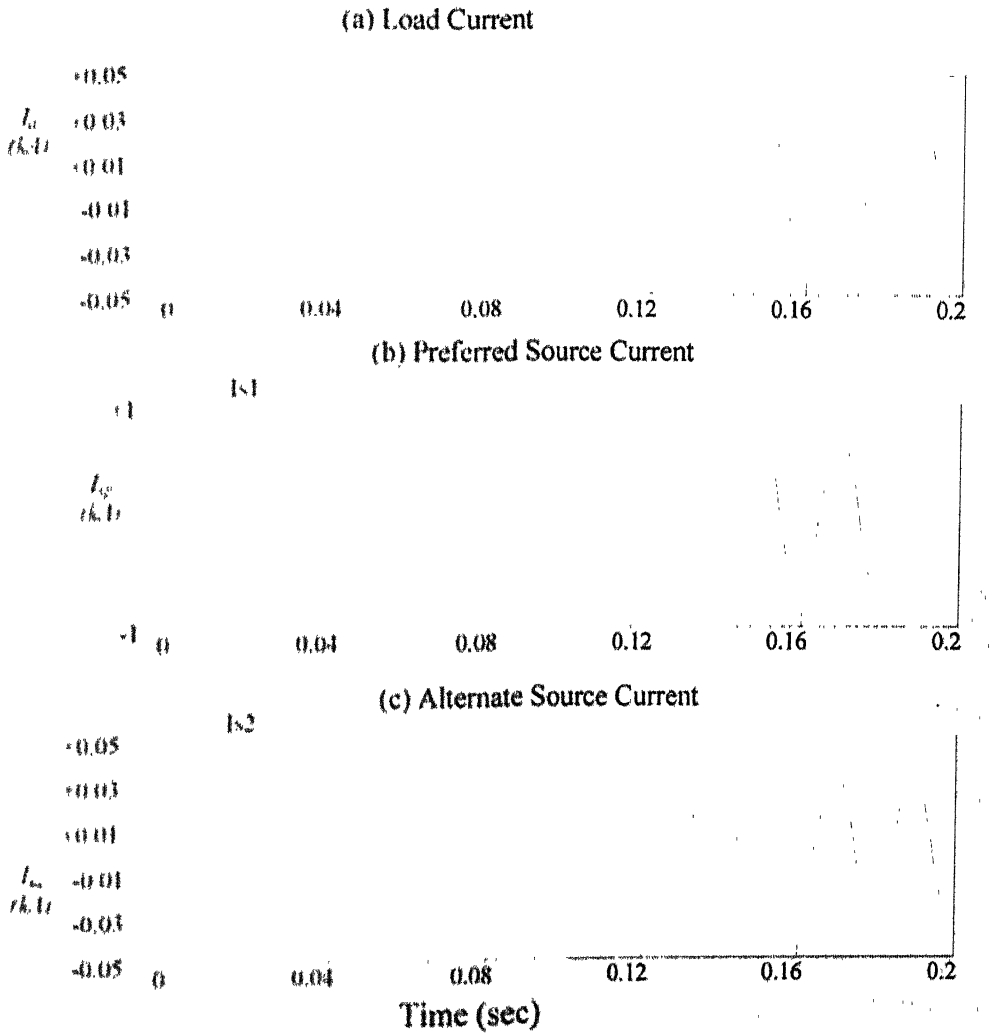

Fig. 2.10. Make-before-break switching system response with SCR based STS

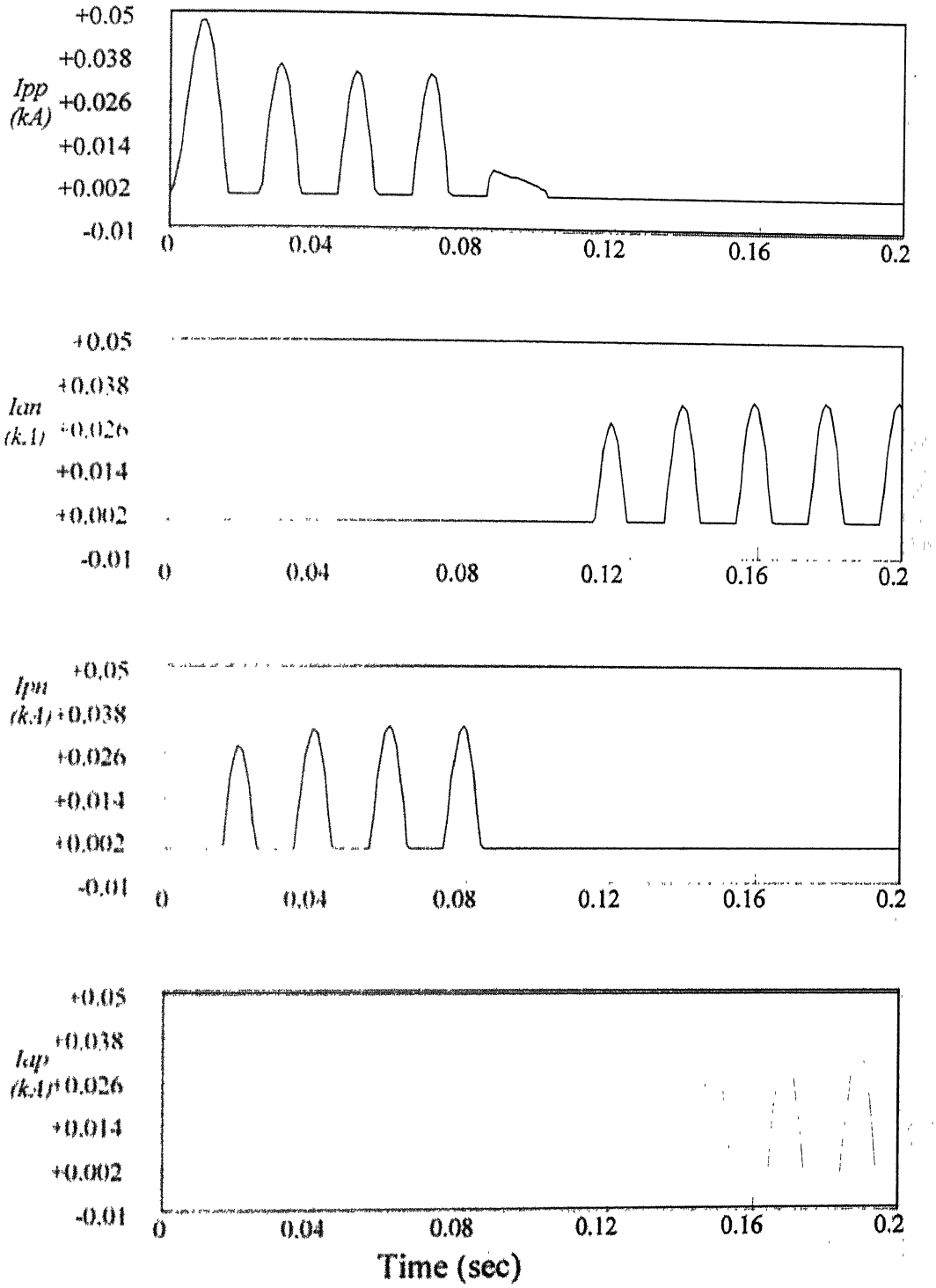

Fig.2.11 Make before-break switching SCR currents of STS

Due to this problem MBB strategy is not applicable for all the operating conditions, as this may lead to temporary transfer of the fault from unhealthy side to

healthy side which cause large current to flow through STS components that is shown in Fig.2.12. The current through each SCR for the incorrect transfer is shown in Fig 2.13. This may damage the STS and destroy the power quality of the sensitive load. To eliminate the possibility of such large current flowing in switches, the transfer in that case has to break before make. This implies that the switching of S_{w2} has to be delayed till the current through out going switch to became zero.

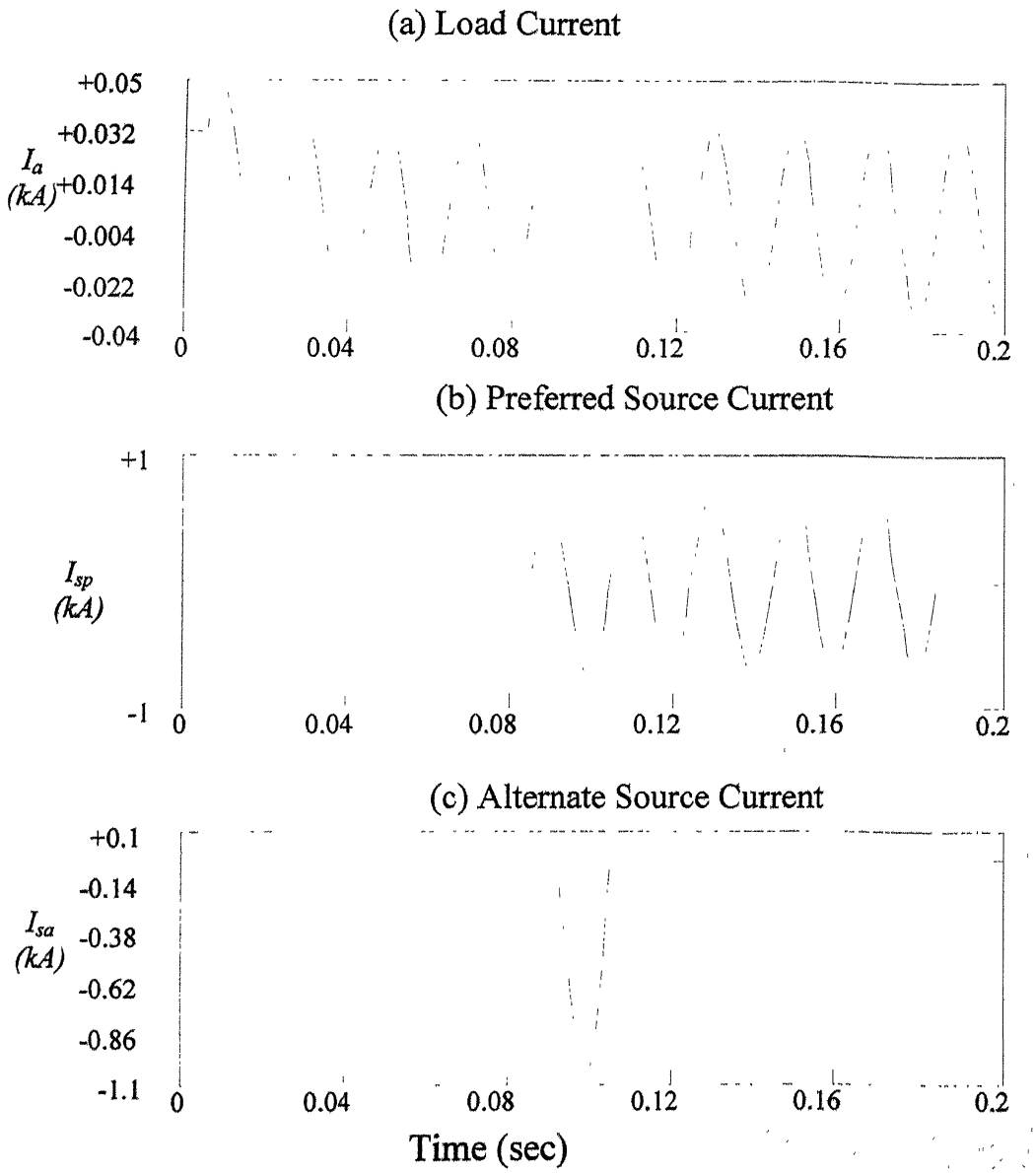

Fig.2.12. Current during incorrect transfer for a fault in the preferred feeder

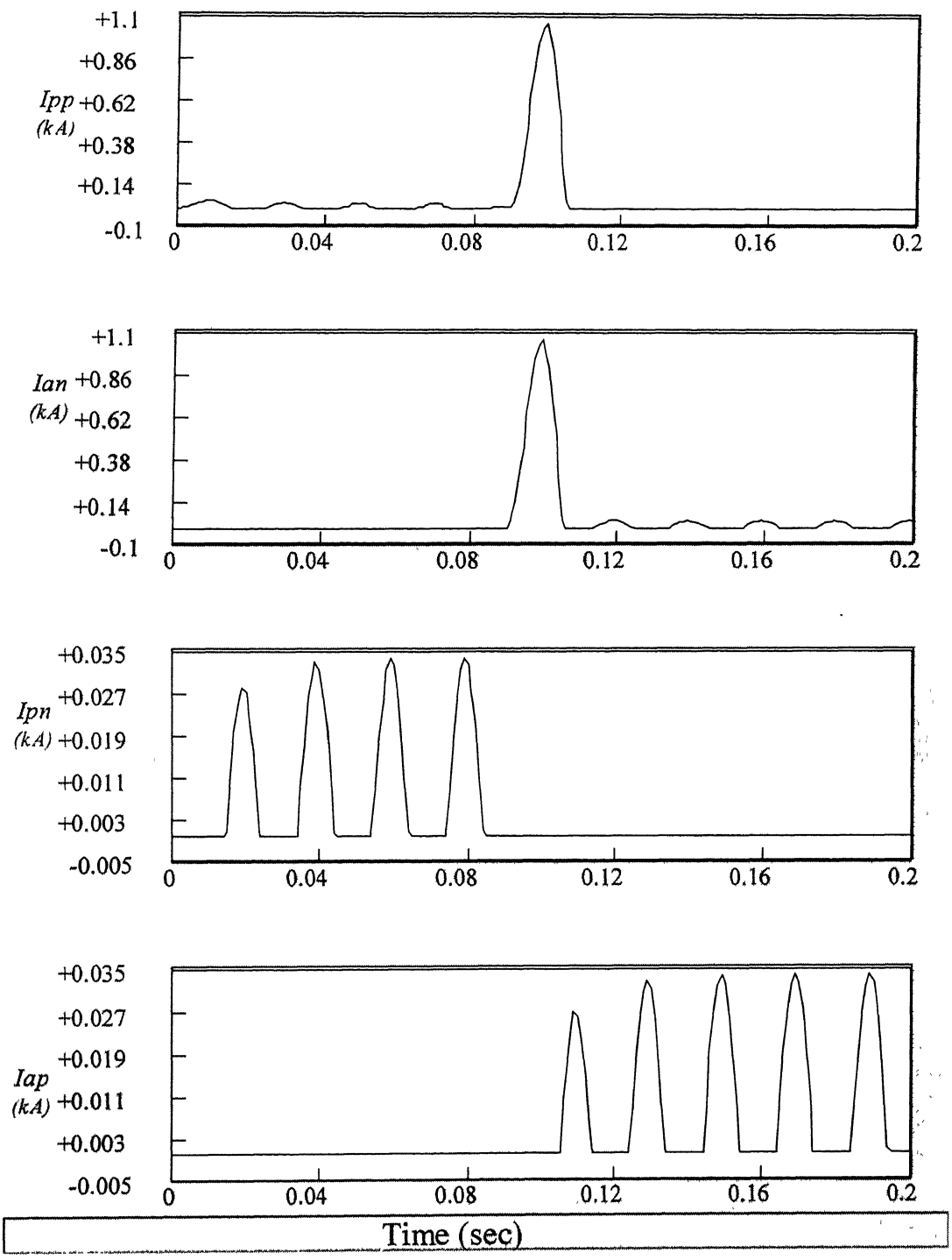

Fig.2.13. SCR currents during incorrect transfer for a fault in the preferred feeder

Simulation result when GTOs are used instead of SCR is shown in Fig. 2.14. The operation is independent of fault instant and other operating conditions. The load

transfer time is 6 ms, which is almost constant for all the switching conditions. This is 2 to 6 ms less than that of the SCR case discussed above.

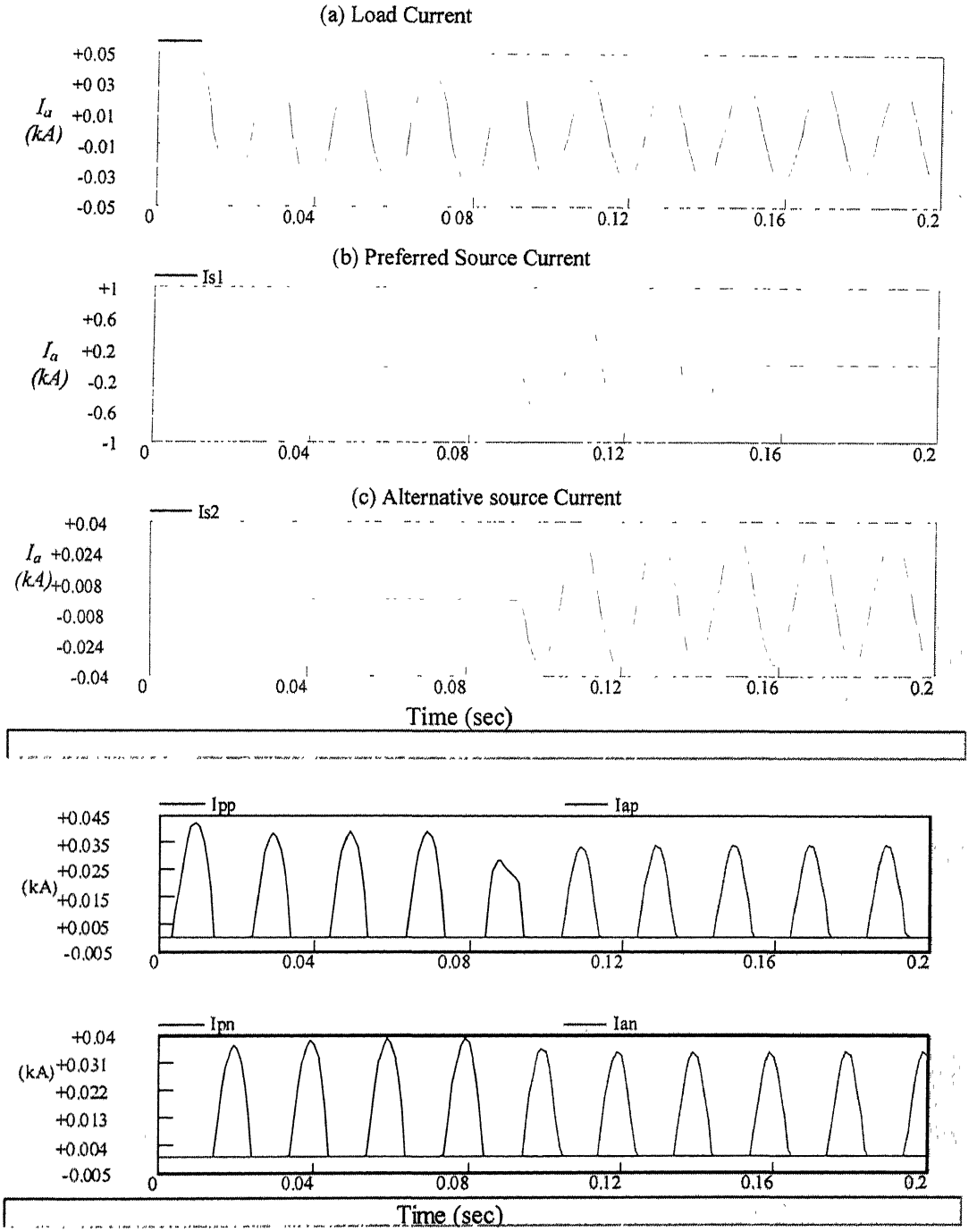

Fig.2.14. Make-before-break switching with GTO based STS

2.7 Conclusions

Topologies of SCL. SCB and STS are presented and function of each component is discussed. Static protective devices are simulated for the simple radial distribution system. The responses of system for different ZnO clipping voltage level are illustrated. The STS is simulated for the single-phase sensitive load. The result is compared for the SCR base topology and GTO based. The later is 2-6 ms faster than previous and more efficient. Thus the working of individual FRIENDS devices is performed with the help of PSCAD/EMTDC software package.

CHAPTER 3

Coordination of FRIENDS Protection Devices

Electromechanical switchgear circuits are still the most common forms of protective devices used in power system. Usually two types of switchgears are used in power system – automatic reclosers and circuit breakers. Automatic reclosers operate for lower current ratings and are placed closer to loads, on feeders or at substations. Circuit breakers are used for higher current ratings and are placed at substations. Reclosers are the first to clear most of the faults. The circuit breakers are used as the second level (backup) protective devices for the case in which the recloser fails to clear the fault. Large current flows through the networks for ground faults. The protective devices must switch off the smallest portion of network without affecting the majority of loads. This objective is accomplished through primary and back up protection using inverse time over current relays. This basic principle of coordination must be kept in mind while placing Static Current Limiter (SCL) and Static Circuit Breaker (SCB).

3.1 Coordination

A generic distribution system is shown in Fig. 3.1 in which the SCL and SCB are placed at positions labeled with numerals. This distribution system has two incoming transformers, each connected to one main bus. These two buses are connected by a bus tiebreaker. As we have observed in Chapter 2 an SCB can interrupt a fault current much faster than an ordinary circuit breaker. Therefore even if the

installation of an SCB in location 1 or 2 will protect the down steam from over current. the coordination of the protective devices will be a major problem unless all protective devices in the network are solid state. Assume that 1 is an SCB while 4 is a conventional one. Then for a fault in the down stream feeder 4, SCB at 1 will operate before breaker at 4 there by disconnecting both faulty and healthy feeder supplied by transformer T_1. This clearly is unacceptable.

A potential installation point of an SCB is the bus-tie location 3, where it operates in a normally closed mode. Since an SCB can clear a fault instantaneously, it can isolate the two systems for a fault in either of the buses. For example, a fault on the left-hand side of the breaker can be isolated quickly such that the transformer T_2 does not feed the fault. The other obvious potential application point of the SCB is location 7, which protects a particular load. A fault on the load side can be quickly isolated by the SCB with out affecting any other part of the system.

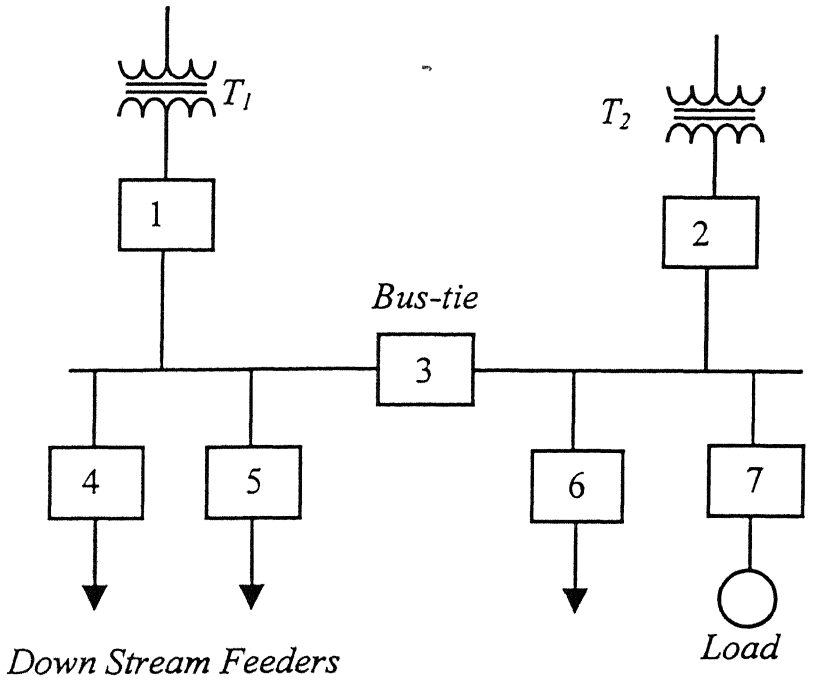

Fig. 3.1 A generic distribution system

The best position for the placement of a static current limiter (SCL) is at the output of the main incoming transformers, i.e. location 1 and 2. This will limit the current for faults in any part of the network. Further more, such an arrangement will not cause any serious coordination problem. The current tap setting of the down stream over current relays can then be set for a lower values. SCL or SCB can also be put on the feeder location 4, 5, and 6. These devices have a lower current rating than those place at 1 and 2.However since these devices are more expensive than the conventional circuit breaker/reclosers, such arrangement obviously will incur much higher cost and may be justifiable only after once the cost-benefit ratios are calculated.

A limiter at the bus tie location 3 can be most benefited, as it will have lower losses under normal operating conditions because less amount of current is supplied via this. However since the current flowing through this position for a fault at any part of the circuit is maximum, the rating of the device at this location must be comparatively high.

3.1.1 Main SCL/SCB Features for Protection Coordination

From the above discussion we can summarize the main features of coordination.

- It must limit the short circuit current such that it does not exceed the momentary or interrupting rating of any down stream protecting devices.
- It must maintain the fault current with in a specified limit till a down streams device clear the fault.
- The limiter must reset automatically after the fault is cleared.
- It must allow sufficient fault current to flow such that it does not interfere within any down stream over current protection device.

- It must relatively free from maintenance.

3.2 Test System

Based on above consideration a test system has chosen for simulation studies. The test system is shown in Fig. 3.2. Generators G_1 and G_2 are supplying power at 19.05 kV (line-to-neutral, rms) to the incoming feeder via 19.05 kV/6.35 kV (line-to-neutral, rms) transformers to the bus 1 and bus 2 respectively. These buses are connected by a Bus-tie SCB 3. The system frequency is 50 Hz. The each incoming feeder has a resistance of 27.225 Ω and an inductance of 346.5 mH while the transformer has leakage inductance of 346.5 mH referred to the primary side. Down stream feeders 4, 5 and 6 each have the sum of feeder and load resistance of 60.5 Ω and inductance of 770.3 mH. The load supplied through SCB 7 has resistance of 30.25 Ω and inductance of 385.15 mH.

This implies that for a base voltage 33 kV (L-L) and a base MVA of 1, the incoming feeder impedance is 0.025 + j0.1 pu and the leakage inductance of the transformer is j0.1 pu. The impedance of each of the downstream feeders 4, 5 and 6 is 0.5 + j2.0 pu and the load labeled 7 impedance is 0.25 + j1.0 pu. The steady state current in the feeders 4, 5 and 6 is 24.30 A (rms), i.e., 0.463 pu. Load 7 draws 48.60 A (rms) i.e. 0.926 pu. If the bus-tie is in closed position, the same amount of current will be supplied by the both sources which is 60.625 A (rms), i.e., 1.1575 pu. By the network topology 12.15 A, i.e., 0.2315 pu current is passing through bus-tie. This power delivery system is simulated in PSCAD/EMTDC software package and proper coordination is achieved in subsequent sections. The PSCAD/EMTDC simulation draft is presented in Appendix B

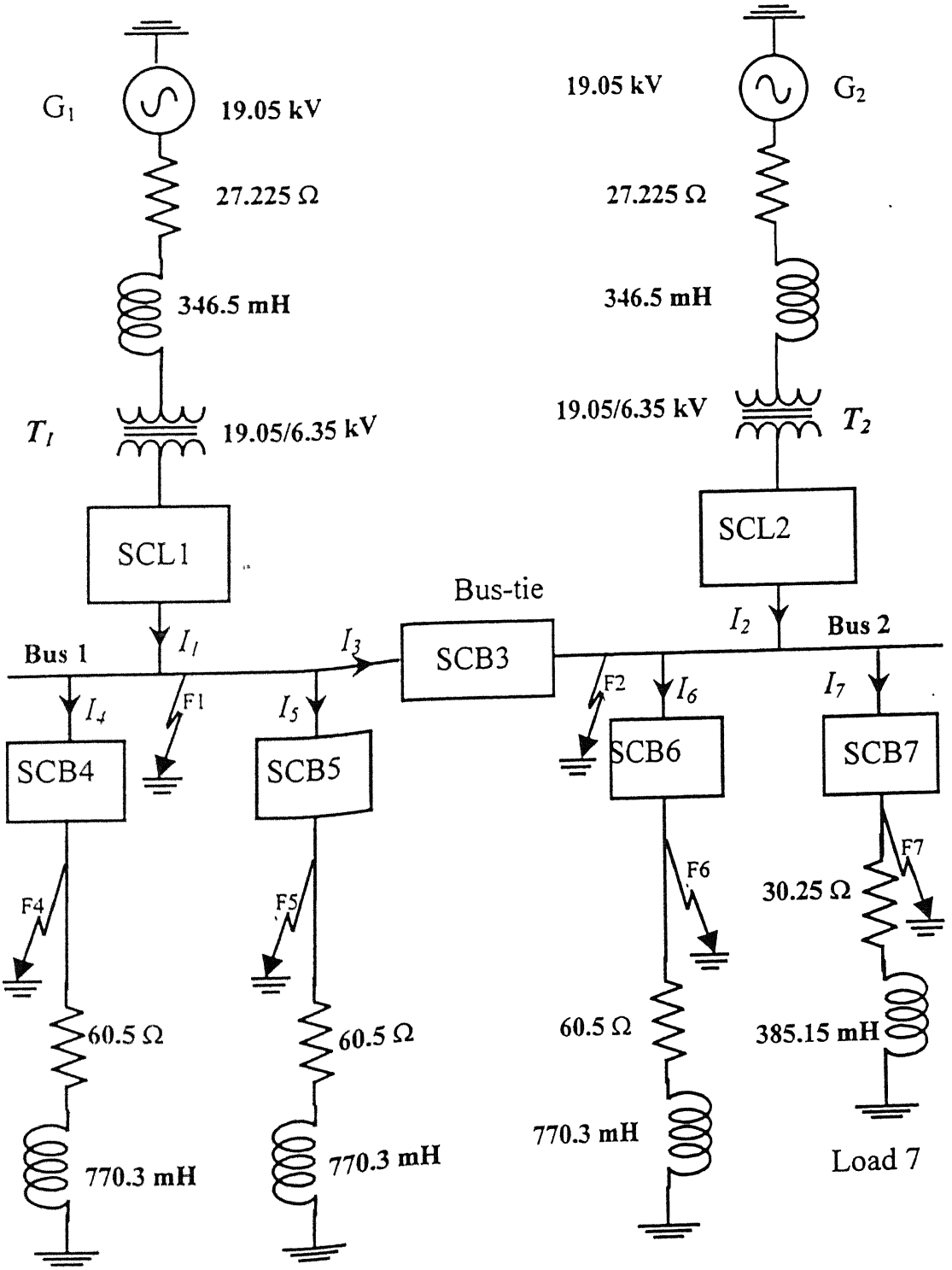

Fig.3.2 Test distribution system

3.3 Control Strategies for PSCAD/EMTDC Simulation

The SCL 1 and 2 provide primary protection for the fault at the bus and back up protection to the down stream feeders and load. Similarly SCB 3 functions differently for bus fault and fault at feeders. For the fault at bus it is compulsory for this to isolate the healthy section from unhealthy section within a short time. But in case of fault at the feeders, which are primarily protected by the SCBs connected to the concerned feeder, SCB 3 provides back protection.

To achieve the goal, The current settings of SCL 1 are chosen to be 120 A (i.e.2 pu) of the normal rms value of the current I_1 as primary protection. For the back up protection of down stream feeders 4 and 5, the current settings are taken as 144 A (i.e. 6 pu) of their normal rms values. The SCLs operate for 5 cycles of the supply. The current setting of SCB 3 are 30 A (2.5 pu) for primary protection and 6 pu of the normal rms current of the corresponding feeder and load for back up protection. The current setting of SCB 4, 5, 6 and 7 are fixed at 2 pu of the normal values of rms currents of the respective feeders and load. The system is simulated with various fault locations. Fault locations, instants and related protection coordination are given in Table 3.1.

3.3.1 Control Strategy of SCLs

The control strategy of SCL 1 is shown in Fig 3.3. The main components of control strategy are Phase Logic Loop (PLL), comparator and setting unit, multi input OR gate and firing unit. The secondary voltage of transformer is given as input to PLL, which generate the reference phase angle for firing unit. The current I_1, I_4 & I_5 are compared with their setting and corresponding signals are generated. Trip signal i_1' is generated corresponding the primary protection of bus 1 and signal i_4'' & i_5'' are for

back up protection of feeder 4 and5 respectively. These signal are sent to firing unit via OR gate. Firing angle setting is done corresponding the load power factor. Firing unit generates triggering pulses to each GTO of SCL 1.

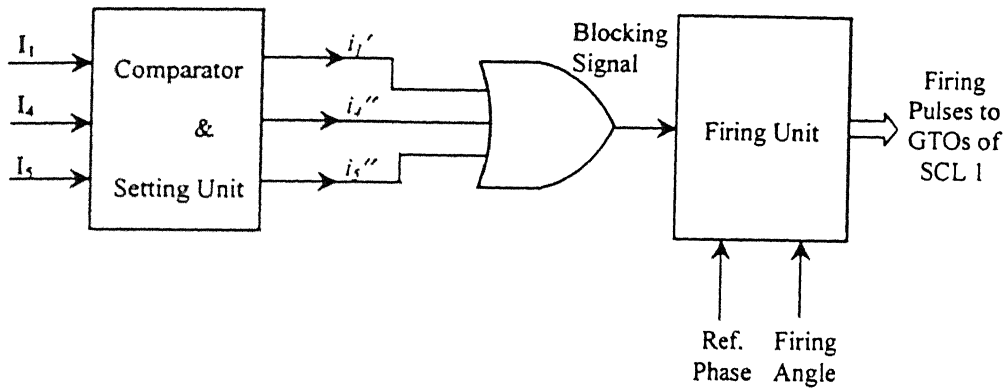

Fig. 3.3 Control strategy for SCL 1

Table 3.1 Various Faults and Coordination of Protection Devices.

Fault	Location	Instant (seconds)	Primary Protection Devices	Pick up Current (Primary)	Back up Protection Devices	Pick up Current (Back up)
F_1	Bus 1	0.11	SCL 1 & SCB 3	2& 2.5pu	-------	-------
F_2	Bus 2	0.12	SCL 2 & SCB 3	2& 2.5pu	-------	-------
F_1 & F_2	Bus 1 & 2	0.115 & 0.153	SCL 1&2 SCB 3	2& 2.5pu	-------	-------
F_4	Feeder 4	0.1197	SCB 4	2 pu	SCL 1 & SCB 3	6 pu
F_5	Feeder 4	0.1197	SCB 5	2 pu	SCL 1 & SCB 3	6 pu
F_6	Feeder 6	0.141	SCB 6	2 pu	SCL 2 & SCB 3	6 pu
F_7	Load 7	0.135	SCB 7	2 pu	SCL 2 & SCB 3	6 pu

3.3.2 Control Strategy of SCB 3

The control strategy of SCB 3 is shown in Fig. 3.4. The main components are PLL, dual comparator and setting unit, multi input logic gates and firing unit. The function of PLL is same as mentioned above. Dual comparator generates primary

protection signals i_3', i_4', i_5', i_6' and i_7' which are able to isolates the buses in case of fault at buses. It also generates signals for the backup protection of downstream feeders in case of failure of their primary protection, i.e., i_4'', i_5'', i_6' *and* i_7''. The required logic diagram is given in Fig. 3.4. Firing unit generates triggering pulses to each GTO of SCB 3.

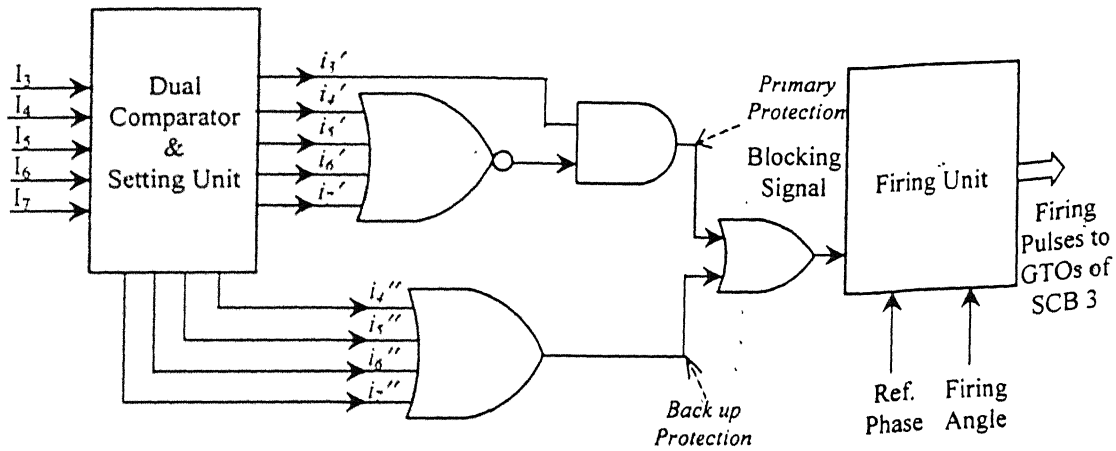

Fig. 3.4 Control strategy for SCB 3

3.4 Simulation Results and Discussion

Steady State response of the Test System simulation result is shown in Fig. 3.5. The system is examined for various unhealthy conditions, which are summarized in Table 3.1. Results for each condition are discussed in subsequent sections.

3.4.1 Fault at Bus 1

The location of fault is shown as F1 in Fig. 3.2. The line to ground fault at bus one is assumed to occur at t = 0.11 second. The system response is shown in Fig. 3.6. The SCL1 respond to the fault within 3 ms and fault current is passed through its let-through (500 mH) inductor and reduced to 0.4 pu. The SCL1 resets to the previous

condition after the 5 cycle of power supply. If fault is still present it will further respond in the same manner otherwise continue in the steady state condition.

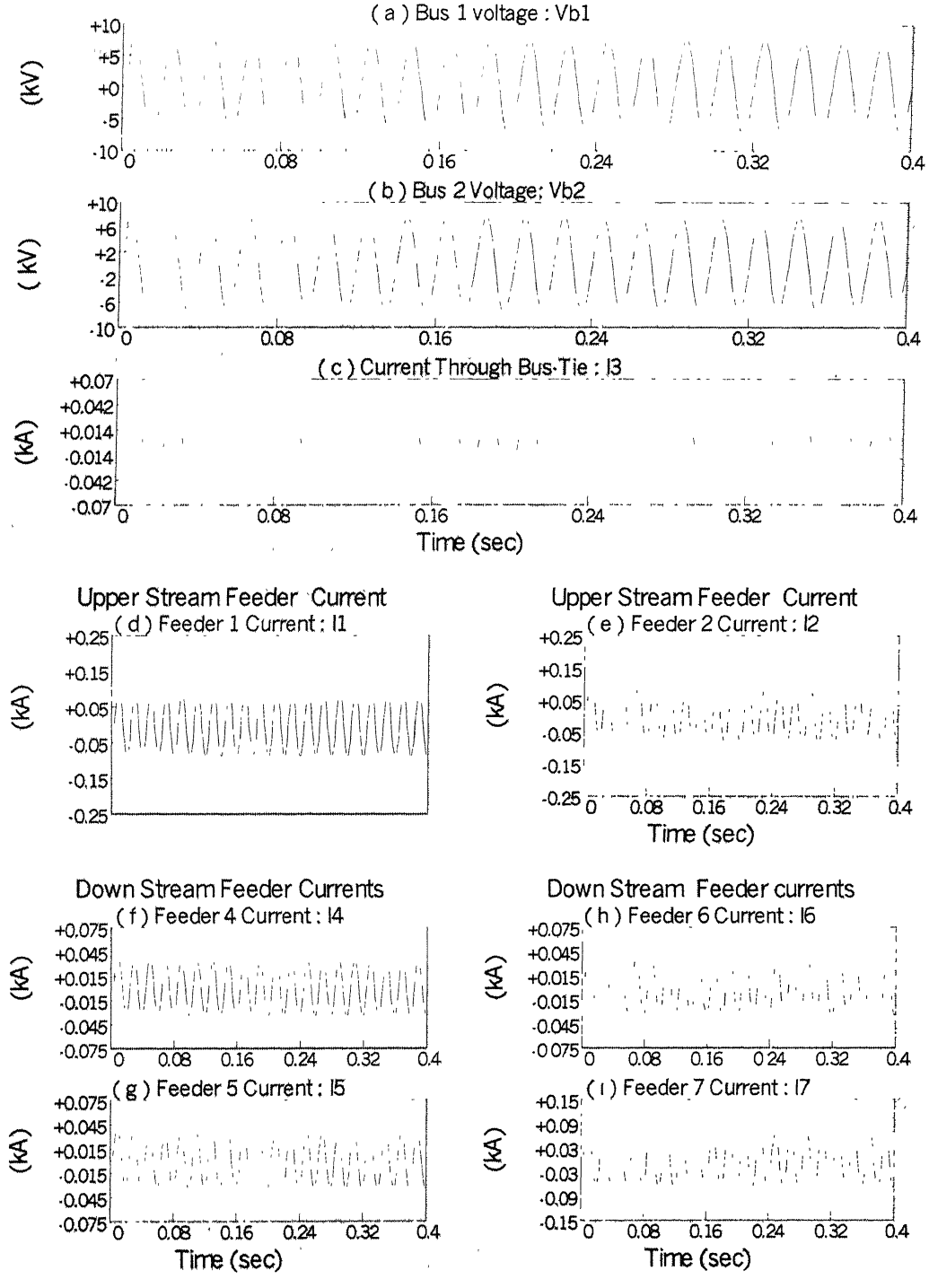

Fig.3.5 Steady state response of the test system

The SCB 3 separates the faulty bus from the healthy one, thus the feeder 6 and load 7 are not affected by the fault. The SCB 3 resets after 10 cycles of the supply. The

portion of power, which was supplied to them by source one is now to be supplied by the source 2 for the next 10 cycle. The currents in feeder 4 and 5 became zero during fault duration. After fault these start to build up but due to the insertion of inductor in the topology current can not reach to the steady state value. After SCL1 is reset at t = 21 ms they are able to rise to rated current.

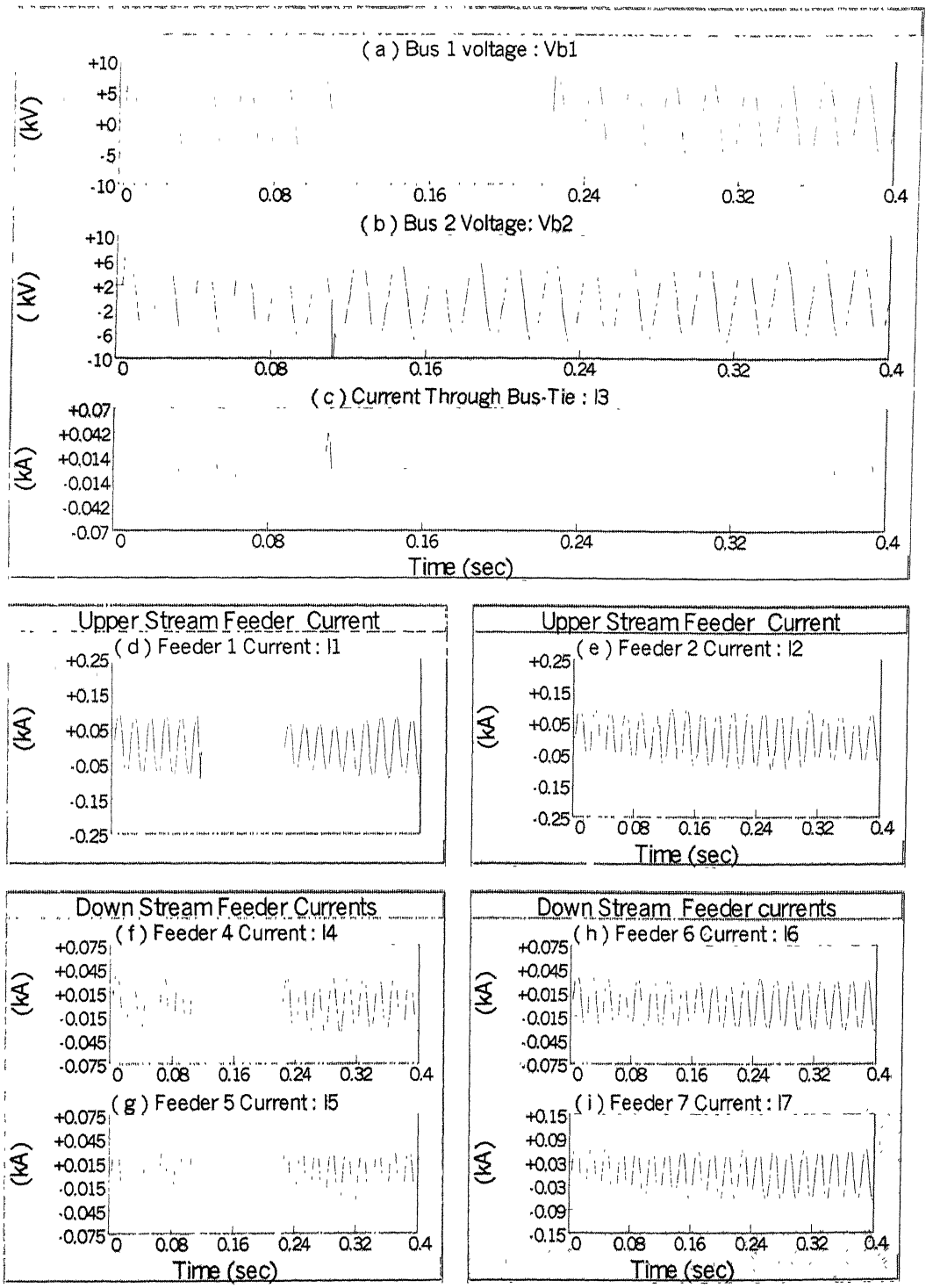

Fig3.6 System response for fault at bus 1

3.4.2 Fault at Bus 2

The location of fault is shown as F2 in Fig. 3.2. The line to ground fault at the bus 2 is assumed to occur at t = 0.12 second. The system response is shown in Fig 3.7. The SCL 2 respond the fault within 3 ms and fault current is passed through its let through (500 mH) inductor and reduced to 0.4 pu. The SCL2 resets to the previous condition after the 5 cycle of power supply. If fault is still present it will further respond in the same manner otherwise continue in the steady state condition. The SCB3 separates the faulty bus from the healthy one, thus the feeder 4 and 5 are not affected by the fault. The feeder 6 and load 7 currents became zero during fault duration. After fault these start to build up but due to the insertion of inductor in the topology current could not reach to the steady state value. After SCL2 is reset at t = 22 ms they are able to rise to the rated current

3.4.3 Fault at both Buses

When the fault at Bus1 occurs at t = 0.115 second and fault at Bus 2 occurs at t = 0 153 second. In this case both the buses simultaneously suffer short circuit fault. Therefore it is not possible to maintain any feeder in healthy state as illustrated in Fig 3.8

3.4.4 Fault at Feeder 4

When fault occurs at feeder 4 it is primarily protected by SCB 4. The system response for this is shown in Fig 3.9 when the fault instant is t = 0.1197 second and pick up current setting of SCB 4 is 2 pu. As mentioned control strategy for SCL 1 and SCB 3, These devices do not response the fault because SCB 4 perform its task faithfully. Thus fault at feeder 4 does not affect any other feeder. This is true for a fault

at any feeder. The power supplied by the source 1 to the feeder 6 and load 7 is now increased due to equal sharing of load via SCB 3.Therefore normal current of SCB3 is considerably increased.

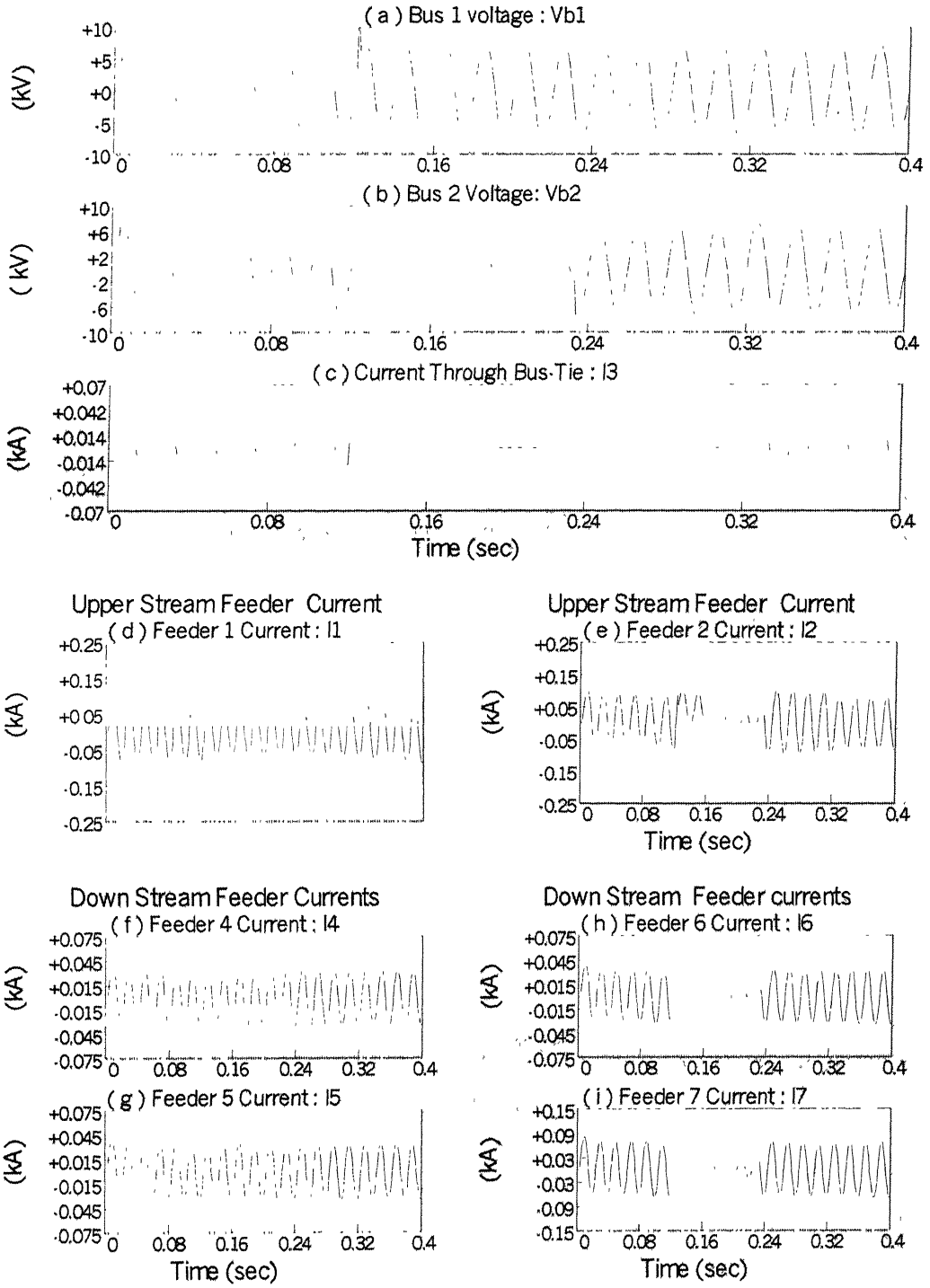

Fig3.7 System response for fault at bus 2

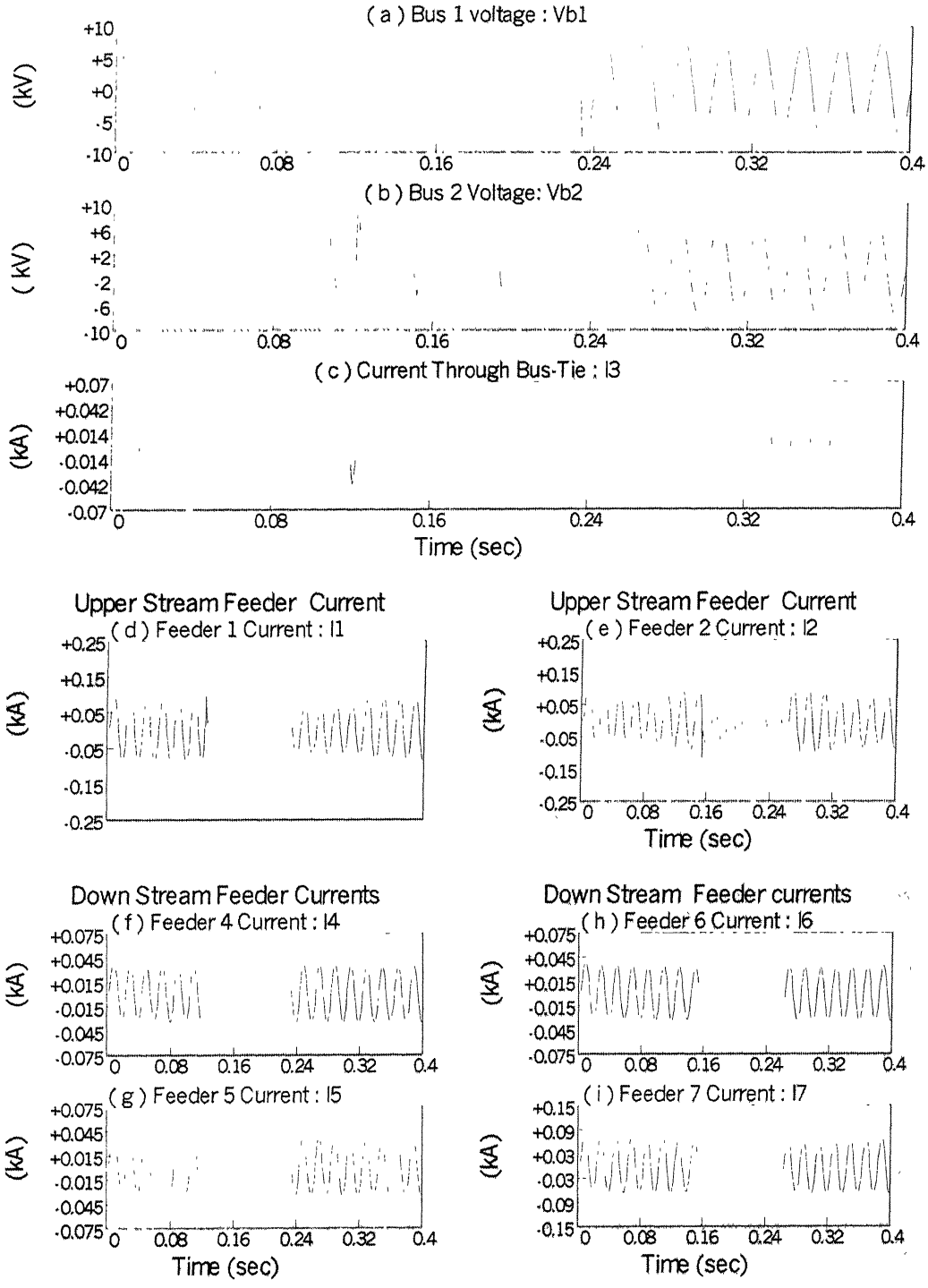

Fig3.8 System response for fault at both buses

In case of primary protection of feeder 4 fails to discriminate the fault, the back up protection is provided by SCL 1 and SCB 3 with 6 pu pick up current setting of the rms value of feeder current. This situation is presented in Fig. 3.10. The fault transfers to source 2 for 2 ms, which activate the SCL 2 for 5 cycle. As SCL 1 and SCB 3 come

into action Bus 2 is separated from fault with in 4 ms. Thus feeder 6 and load 7 are not much affected but feeder 5 severely affected.

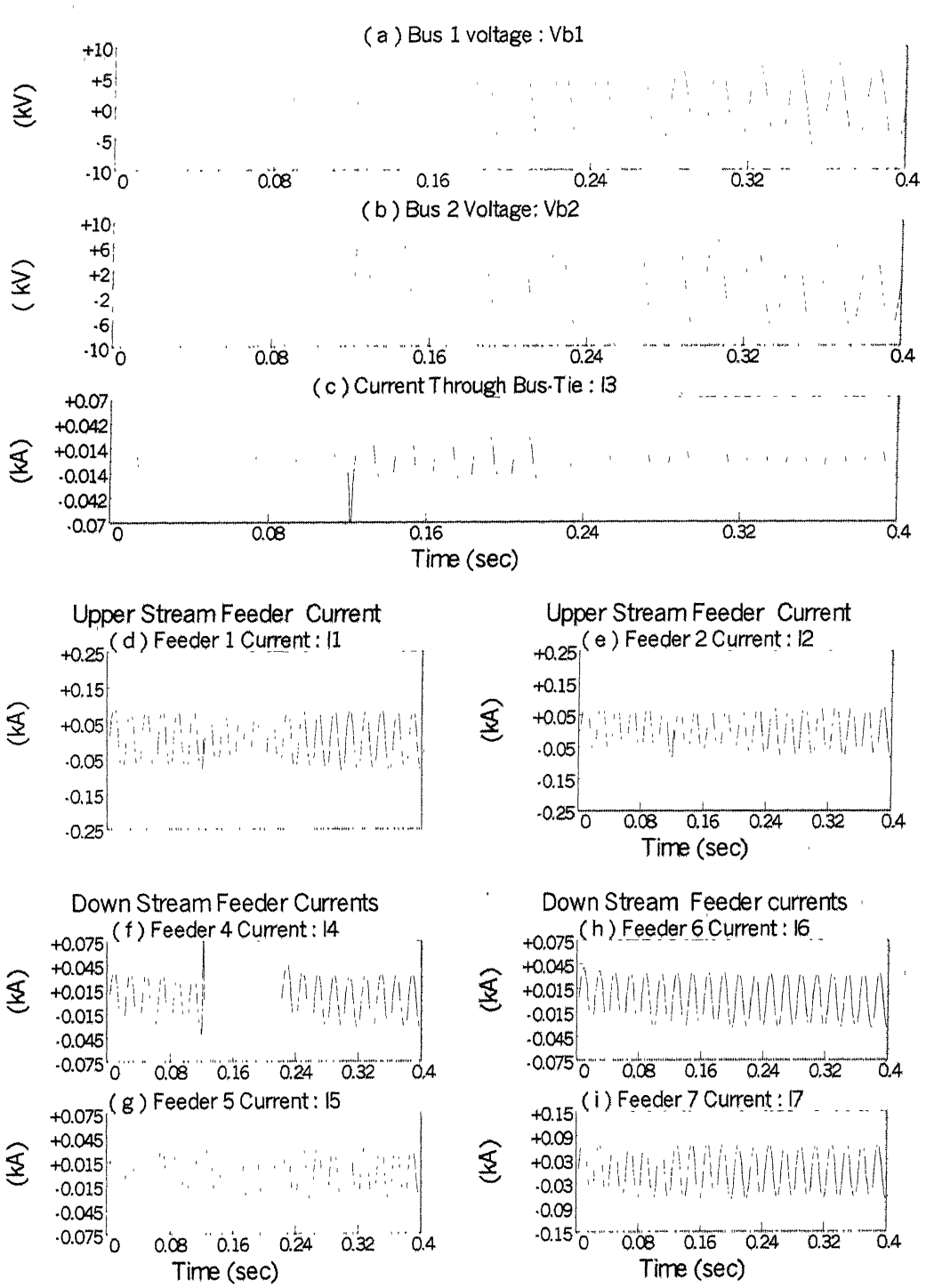

Fig 3.9 System response for fault at feeder 4

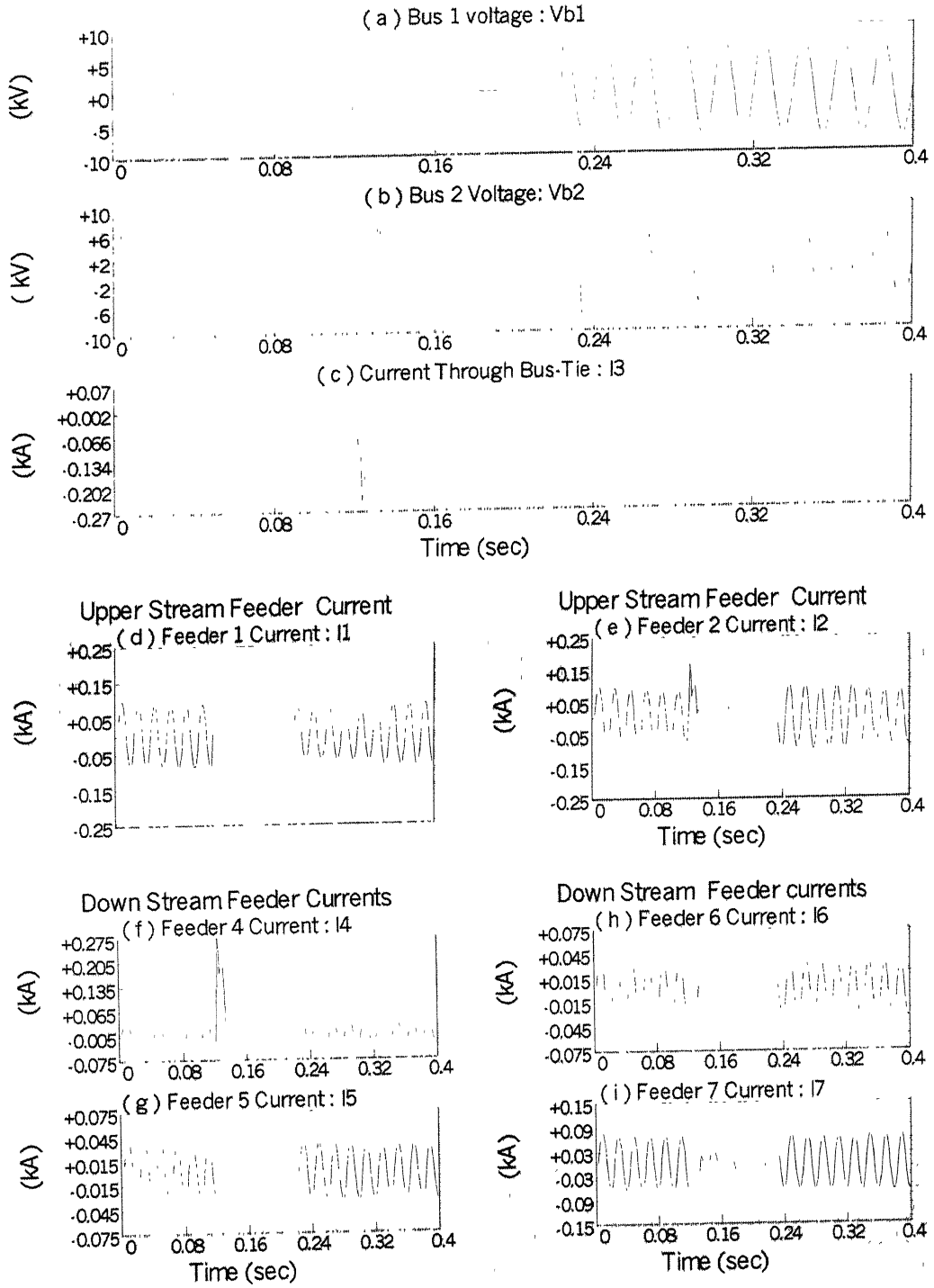

Fig 3.10 System response for fault at feeder 4 with primary protection failure

3.4.5 Fault at Feeder 6

Fault at feeder 6 at t = 0.141 second is consider and simulation result is illustrated in Fig 3.11. In this case SCB 6 takes action and disconnect the load from the

network. The SCB 3 does not operate but due to equal load sharing current through it becomes zero till the fault clearing.

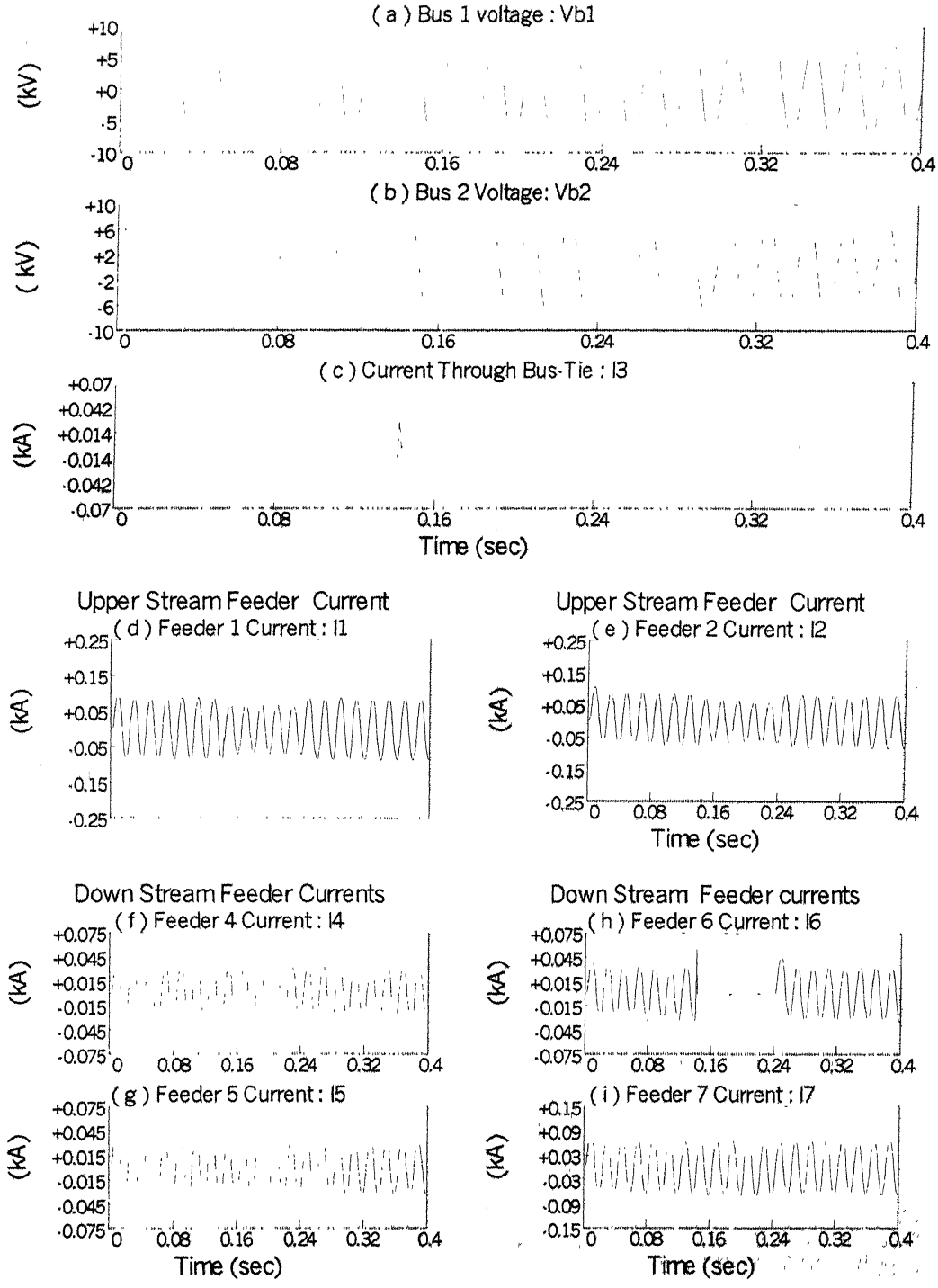

Fig 3.11 System response for fault at feeder 6

3.4.6 Fault at Load 7

Fault at load 7 at t = 0.135 second is considered and simulation result is illustrated in Fig 3.12. In this case SCB 7 takes action and disconnect the load from the network. The SCB 3 does not trip and allows the current to flow, but in the reverse direction. Thus source 2 supplies to feeder 6 and partly to feeders 4 and 5.

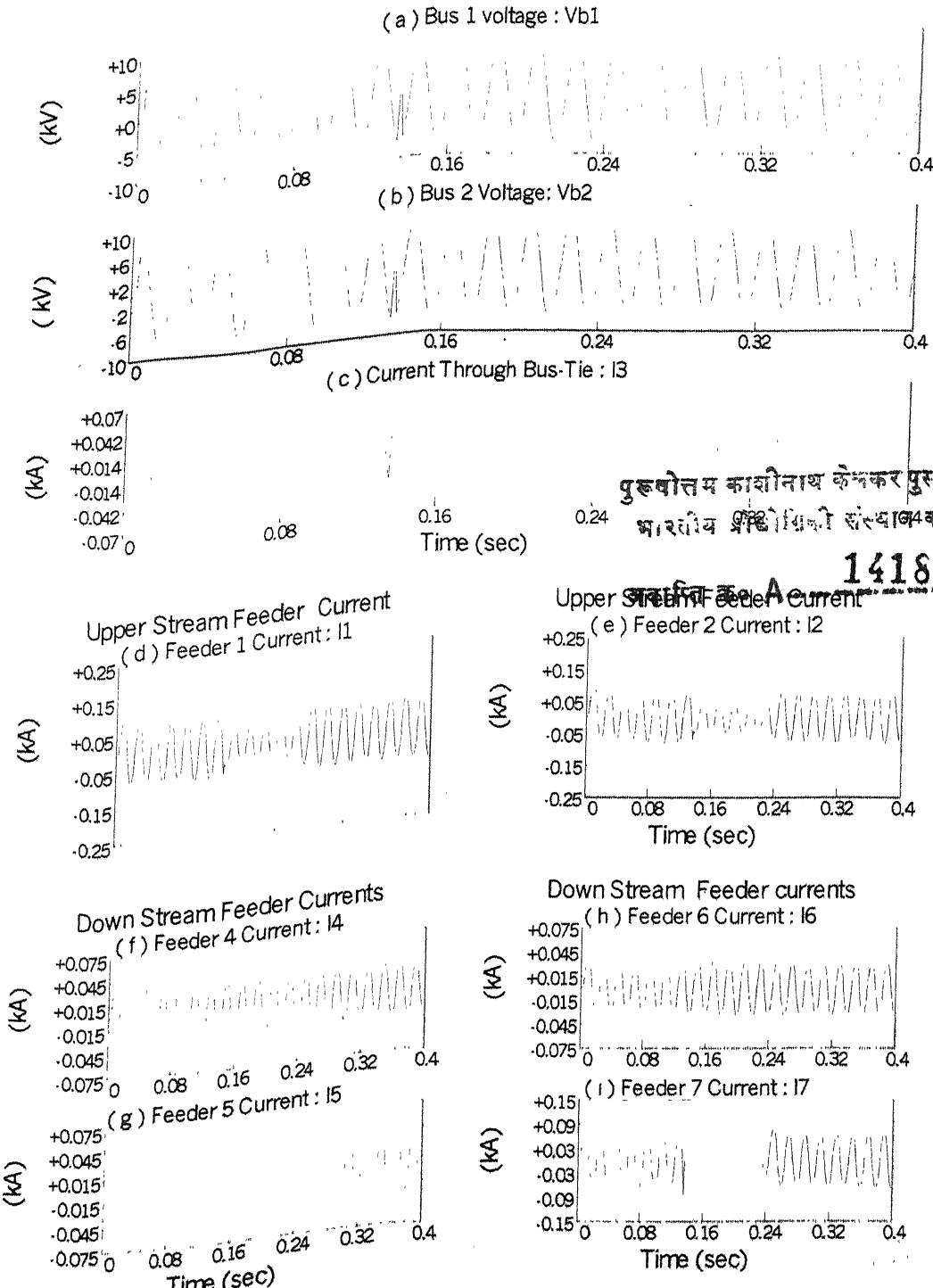

Fig 3.12 System response for fault at load 7

5.5 Conclusions

The coordination problems of FRIENDS devices are discussed with their possible solution. For a generic test system, the proposed coordination is simulated with the help of PSCAD/EMTDC software. Results for different fault cases are illustrated in detail.

CHAPTER 4

Three-Phase Static Transfer Switch

Power quality issues are currently receiving a great deal of attention in the light of distributed generation, deregulation, liberalization and privatization of the electrical energy market. The STS is an important FRIENDS device. The STS has been widely used in low-voltage applications. Availability of reliable semiconductor based switches and stringent voltage quality requirements of sensitive loads have led to medium-voltage applications of STSs during the last few years. The basic idea of STS has been discussed in Chapter 2. Design and performance evaluation of a STS system requires detailed analysis of the supply system and sensitive load. In Chapter 2 an STS that protects single-phase load has been simulated and its performance has also been evaluated. In this Chapter, it is further studied for three-phase applications with active and passive loads.

4.1 Principle of Operation of Three-Phase STS

The schematic diagram a three-phase STS system is shown in Fig. 4.1. The system is composed of:

- A load which is sensitive to variations of utility supply.
- Two independent sources one of which is the preferred one and the other is the alternative one.

- Two three phase thyristor switches T_1 and T_2 which connect the load to the power sources, and
- A control logic to monitor voltage quality of both sources, detect voltage fluctuations in the system, compare the two source and perform a load transfer from one source to another one if needed.

The STS blocks T_1 and T_2 each contain three thyristor modules corresponding to the three phase of the system. Each thyristor module includes two anti-parallel thyristor switches (T_{1p}/T_{1n} and T_{2p}/T_{2n}). Under normal operating conditions, i.e., when the preferred source meets load voltage requirements, the control logic triggers only the thyristors of T_1. If the preferred source can not meet voltage requirement, the control logic will transfer the load to the alternate source if it is in a better condition than the preferred one. This is achieved by removing gating signals from T_1 thyristors and triggering T_2 thyristors. In case of voltage recovery, the load is transferred back to the preferred source. Input signals in Fig. 4.1 are those required for controlling the STS operation. To offer ride-through capability, the load must be transferred within the shortest possible time. Therefore the three-phase STS must meet the following requirements.

- It must detect voltage fluctuations in the system as fast as possible.
- In case the preferred source fails, it must perform a fast load transfer to the alternative source.
- The gating strategy, which controls the transfer process, must prevent paralleling the two sources.

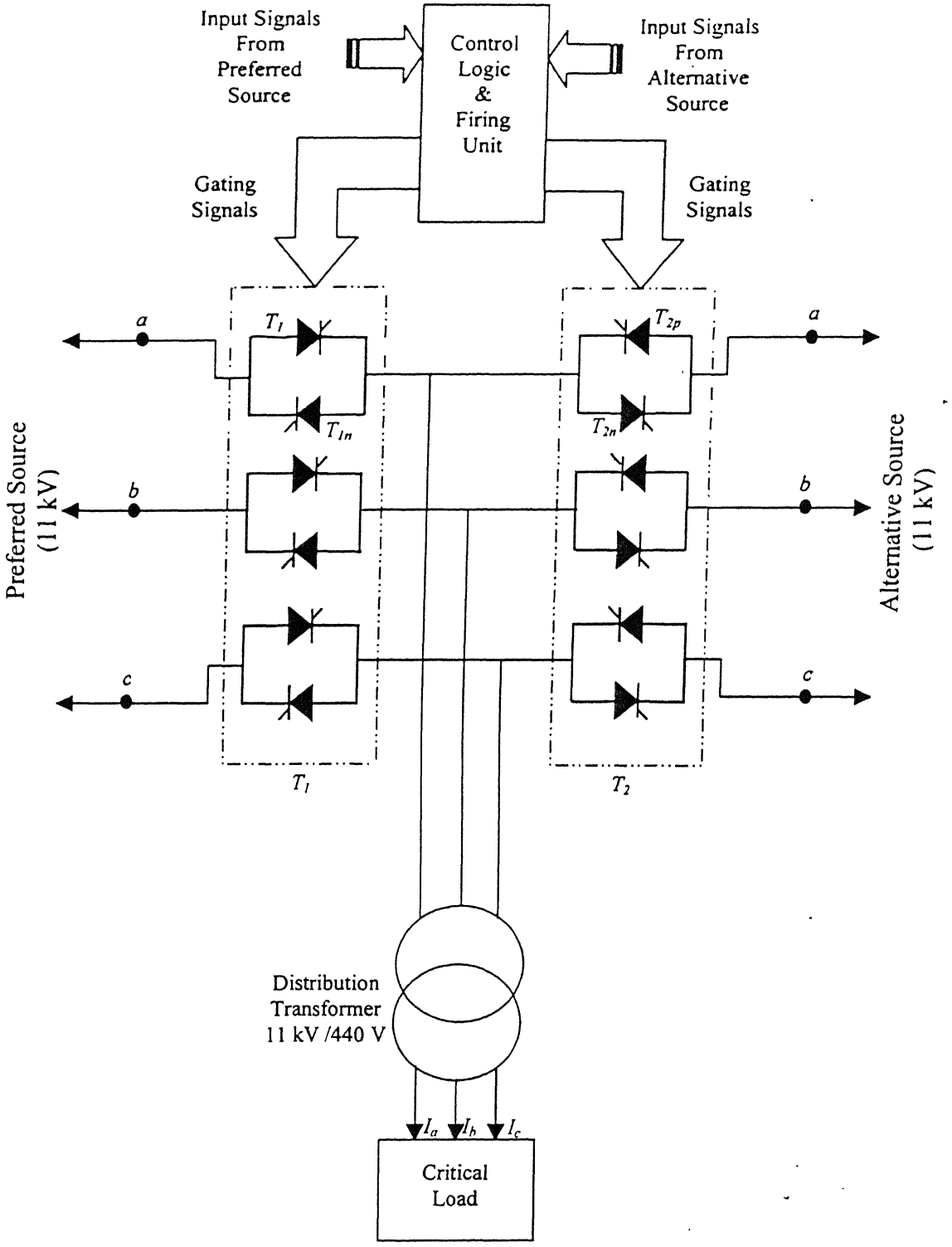

Fig.4.1 Three-phase STS system structure

- Detection and transfer logic must function properly for all possible operating conditions.

- Detection scheme must not be sensitive to temporary voltage transients, e.g. capacitor switching.

4.2 Test System

IEEE benchmark test system [15] is considered here for simulation purpose. It composes of a power circuit and control logic. The power circuit of STS test system consists two 11 KV distribution feeders as preferred (p) and alternate (a) sources. The sources are represented by ideal voltage sources in series with lumped resistances and inductances. The combination of load and distribution transformer is connected to the sources through thyristor blocks T_1 and T_2. Control logic of the three-phase STS is composed of a voltage detection and a gating strategy section. Parameters and functions of each section of the benchmark system are explained in the following sub-sections.

4.2.1 Parameters of STS Benchmark System

Preferred and alternate source systems:

11 kV, 50 Hz

Source resistance and Impedance

$R_p = R_a = 0.015\ \Omega$, $X_p = X_a = 3.6\ \Omega$

Three Phase Δ/Y load transformer

11 kV/480 V, 1 MVA, 50 Hz

Leakage Reactance = 12%

Resistance representing winding losses = 1.5 %

Resistance representing core losses = 0.5 %

Each pair of thyristor valves has a snubber circuit composed of R = 1 MΩ and 001 μf (Impact of snubber circuit on the STS system is insignificant).

The load system is composed of a three-phase RL load in parallel with an induction motor. The series RL load has the following parameters:

$R_l = 0.402\ \Omega,\ X_l = 0.225\ \Omega$

The motor load is rated at:

440 V, 500 kVA, 50 Hz, 2900 rpm

The other parameters of the motor are:

Inertia constant H = 1 second

Stator resistance = 0.33 p.u.

First cage resistance = 0.2 p.u.

Second cage resistance = 0.018 p.u.

Stator unsaturated leakage reactance = 0.098 p.u.

Mutual unsaturated reactance = 3.1 p.u.

rotor unsaturated mutual reactance = 0.1 p.u.

second cage unsaturated reactance = 0.105 p.u.

mechanical damping = 0.008 p.u.

Control circuit parameters are:

$V_{ref.}$ = 16.97 kV

Thyristor turn –off time = 4.8 A

Sampling rate = 6660 Hz

4.2.2 Voltage Detection Strategy

Fig.4.2 shows a block diagram of the voltage detection scheme. The logic is based on transforming ac voltage into a synchronously rotating frame (abc-to-dq0) based on equation (1).

$$v_{dq0_p} = K_s v_{abc_p} \tag{4.1}$$

where

$$v^T_{dq0_p} = \begin{bmatrix} v_{q_p} & v_{d_p} & v_{0_p} \end{bmatrix}$$
$$v^T_{abc_p} = \begin{bmatrix} v_{ab_p} & v_{bc_p} & v_{ca_p} \end{bmatrix}$$

$$K_s = \begin{bmatrix} \cos\theta & \cos(\theta - 120^\circ) & \cos(\theta + 120^\circ) \\ \sin\theta & \sin(\theta - 120^\circ) & \sin(\theta + 120^\circ) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$$

$$\theta(t) = \int_0^t \omega(\xi) d\xi + \theta(0).$$

In this equation

$v_{ab_p}, v_{bc_p}, v_{ca_p}$ are Preferred-source voltages

$v_{d_p}, v_{q_p}, v_{0_p}$ are dq0 component of preferred source in the synchronously rotating frame

ω is angular frequency of the rotating frame

$\theta(0)$ is initial value of θ

The peak value of v_{d_p} and v_{q_p} are calculated as :

$$v^r_p = \sqrt{v^2_{d_p} + v^2_{q_p}} \tag{4.2}$$

The output of the transform action block, v^r_p (given by equation 4.2) is compared to a dc reference, i.e., V_{ref}. Output of the comparator is given to monostable,

which generates a transfer signal. The transfer signal initiates a transfer process if the preferred source fails to provide the required power quality.

4.2.3 Gating Strategy

The gating strategy is composed of three identical sets of logic for the three phases of the system. It provides selective gating patterns to thyristor switches which result in a fast load transfer process and prevent source paralleling. The selective gating strategy is based on the direction of line current flow. Fig. 4.3 shows the gating logic diagram which is consists of the following blocks.

Current direction detection logic is responsible for detecting the status of the thyristor switches, i.e., on/off state and selecting the right switch to trigger to prevent source paralleling during the transfer process. *Phase logic Loop and Firing Angle Controller* sets the firing instant according the load voltage waveforms. If the GTOs are used current waveforms are also to be considered.

Gating-pattern generation logic generates selective gating signal for both T_1 and T_2 thyristors switches. For normal operation gating signal are generated for T_1. When load transfer signal is received from the voltage detection unit, it will stop the gating signal for T_1 and start for T_2 according to the status of T_1 thyristors. For example, if T_{1p} (outgoing switch) is conducting at the time and a disturbance is detected. The transfer process begins with triggering T_{2p} and not with T_{2n} as T_{1p} is in on state. During the transfer operation, two scenarios may occur in each phase. The first scenario is when commutation begin as soon as the incoming thyristor, e.g., T_{2p}, is gated. This is make before break (MBB) strategy. The preferred source current drops and the alternate source current increases to the load current.

The second scenario occurs when commutation fails (e.g., T_{2n} is gated) and the out going thyristors continue conducting until a zero crossing is reached and natural commutation begins. MBB is not allowed for this scenario and break before make (BBM) strategy is followed. These strategies are explained in Chapter 2 in detail. The thyristor turn off time is also considered before gating incoming thyristor, e.g. T_{2n} to make sure that the outgoing thyristors have regained their blocking capability

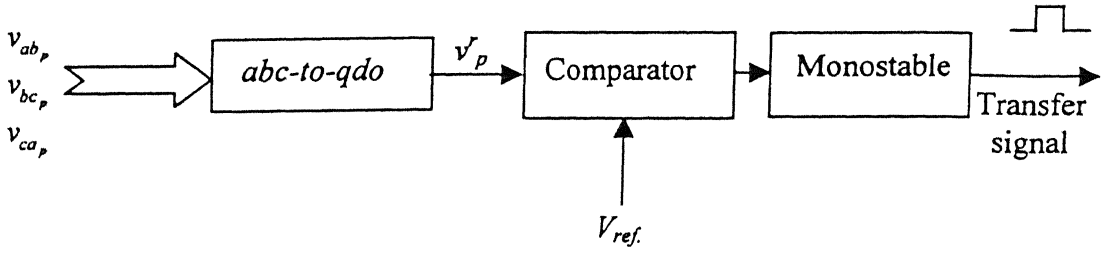

Fig.4.2 Block diagram of voltage detection scheme

4.2.4 The STS system Terms and Definitions

Definition of detection, transfer and total load-transfer times are as follows according to IEEE standard [15]:

- ***Detection Time:*** The difference between the time at which a disturbance occurs and the time at it is detected.
- ***Transfer Time:*** The difference between the time at which a disturbance is detected and the time at which the last faulty phase is transferred.
- ***Total load-transfer time:*** The sum of detection time and transfer time.

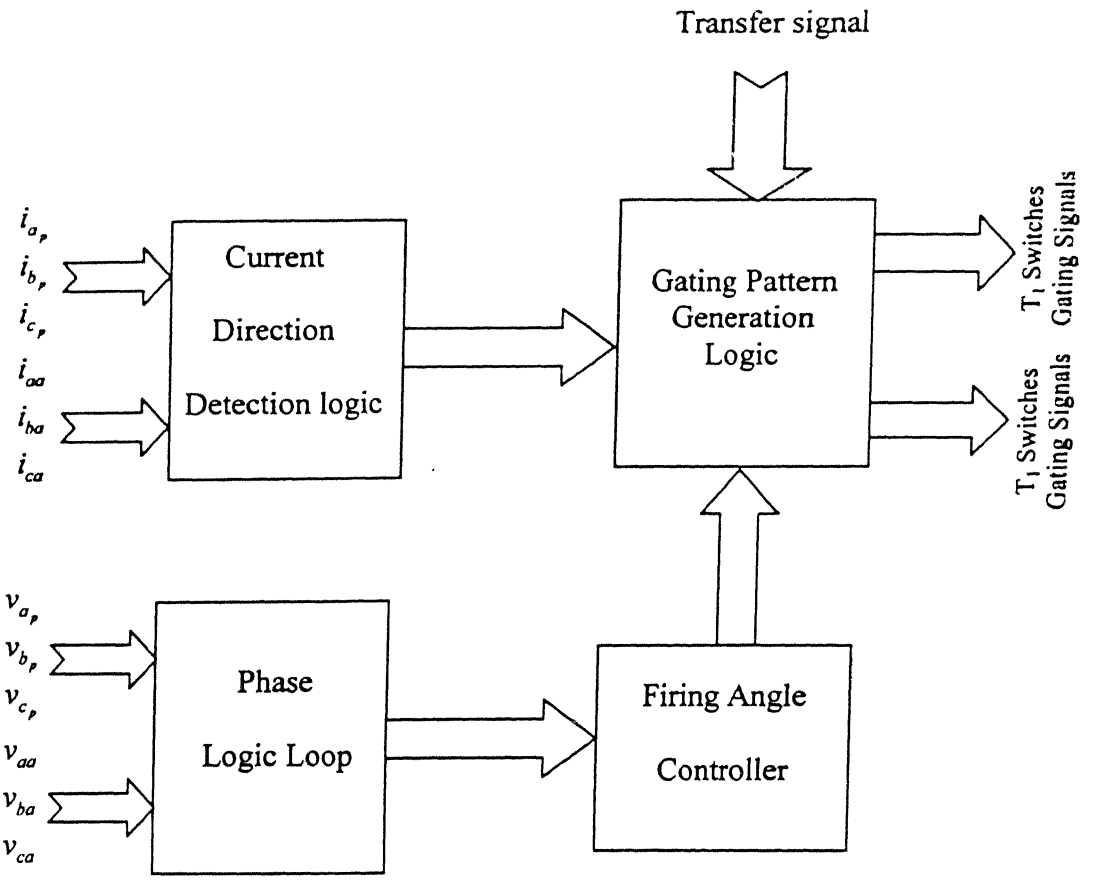

Fig.4.3 Block diagram of gating scheme

4.3 Simulation Results and Discussions

The simulated performance of the STS benchmark is presented in the subsequent sub-sections for passive and active loads. These simulations are performed by PSCAD/EMTDC software package in which undervoltage disturbances are created by simulating various types of faults on the preferred source terminals.

4.3.1 Passive R-L Load

The threshold of voltage detection unit (Vref, Fig. 4.2) is set as 75% of systems nominal voltage. The simulated result for three-phase fault condition is shown in Fig. 4.4. Three phase to ground fault is created at 0.1195 second, which is detected at 0.121 second. Thus the detection time is 1.5 ms. The load is transferred at 0.129 second, i.e.,

the transfer time is 8 ms. The total transfer time is the sum of these two and is 9.5 ms. It is expected that this would not affect the performance of a sensitive load. The voltage transformation block output, i.e., v'_p (Fig. 4.2) sharply goes to zero for three-phase to ground fault and it remains zero till fault is cleared as shown in Fig. 4.4.

Avoidance of cross-current: A condition of maloperation is represented in Fig. 4.5, when on/off status of out going thyristors of block T_1 is not considered in the transfer process. This leads to paralleling in the phase A of the preferred and the alternative sources. This is known as cross current phenomenon. However the transfer process of phases B and C completed without paralleling. This depends on the power factor and the instant of fault. The paralleling occurs for a short time that is less than half cycle of the supply. The peak of the phase current during the paralleling is 6 kA and that may damage both incoming and outgoing thyristors simultaneously.

Two phase to ground fault is also simulated for the same load and operating conditions. Here the threshold of voltage detection unit is set at 80% of the normal voltage. Simulation result is shown in Fig. 4.6. In this case the output of the voltage transformation block is not a DC value and it does not go to its minimum value sharply. Thus detection time is increased to 2.1 ms. Similar result for single-phase to ground fault is presented in Fig. 4.7. The detection time here is 2.5 ms.

4.3.2 Regenerative Load

Simulation result for three phase induction motor load is shown in Fig.4.8 for two phase to ground fault. The detection time is observed to be 2 ms and the transfer time is 8.5 ms. The transfer time has a large value as compared to the passive load. The reason for this is that the load feeds the fault through T_1 thyristors, and the transfer cannot be completed until current through out going thyristor becomes zero. This is

observed in phases B and C, which are subjected to fault. The current throughout going thyristors is governed by the regenerative load in Fig. 4.8.

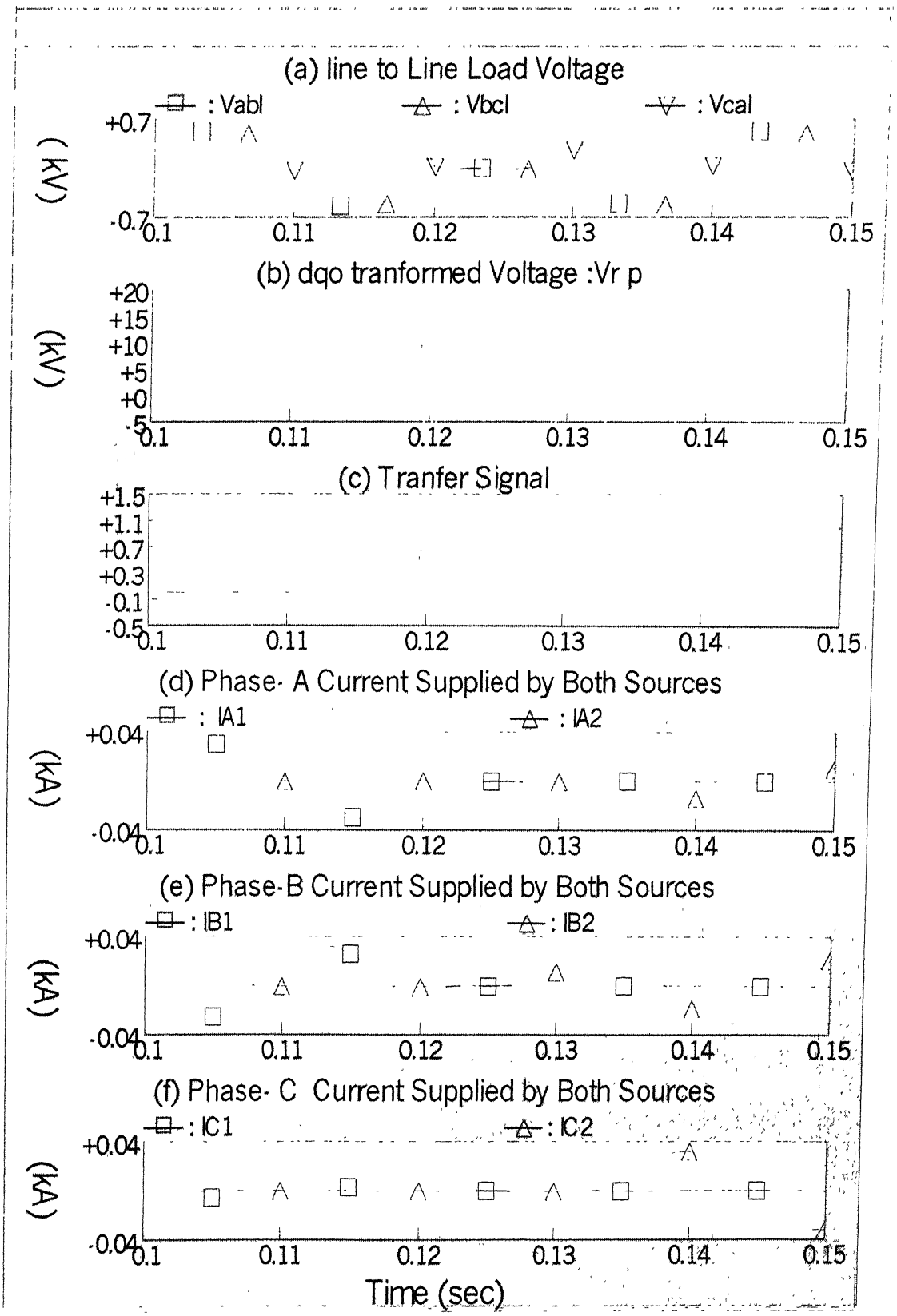

Fig. 4.4 R-L load, three-phase to ground fault, system response

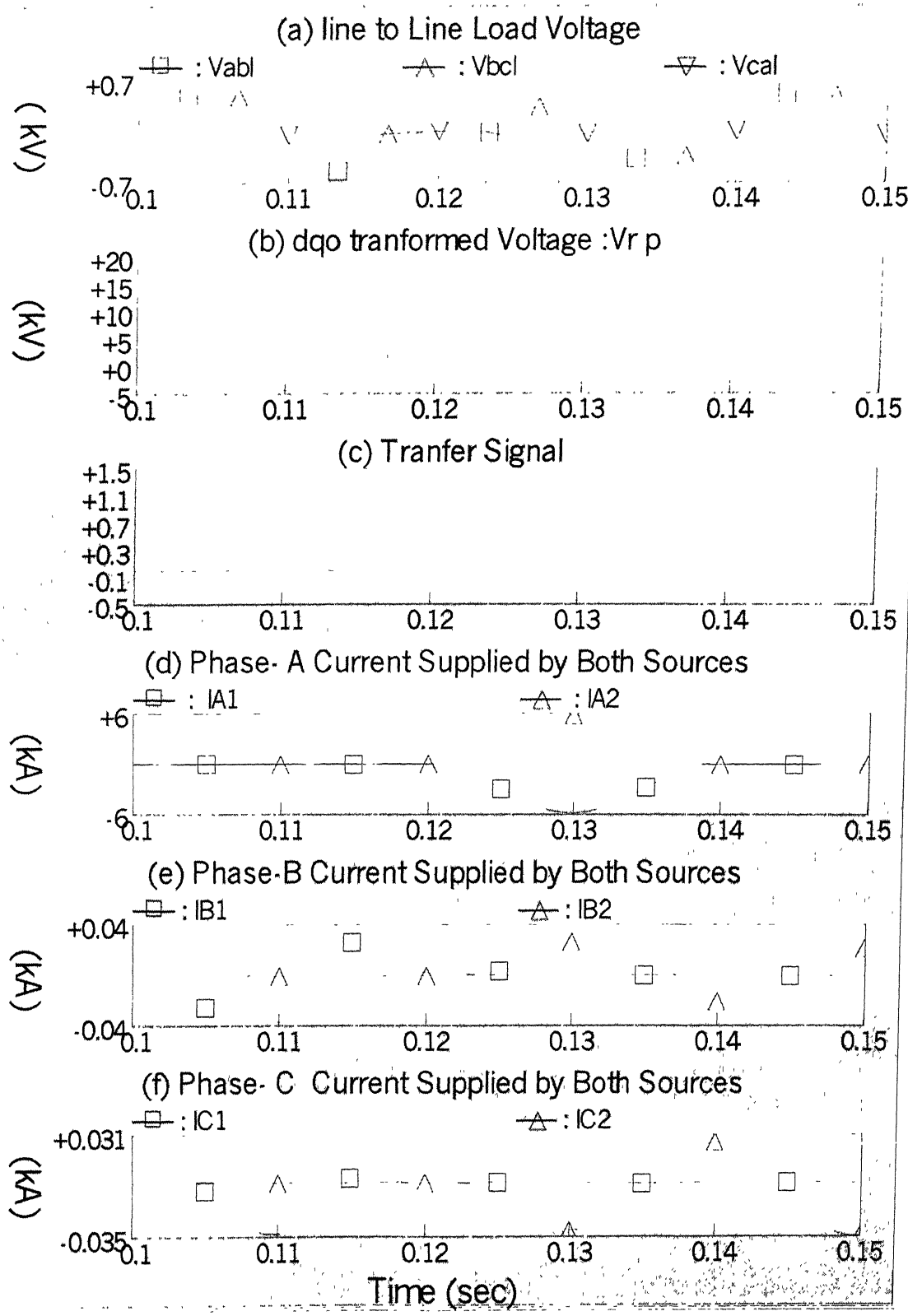

Fig. 4.5 R-L load, three-phase to ground fault, cross current phenomenon

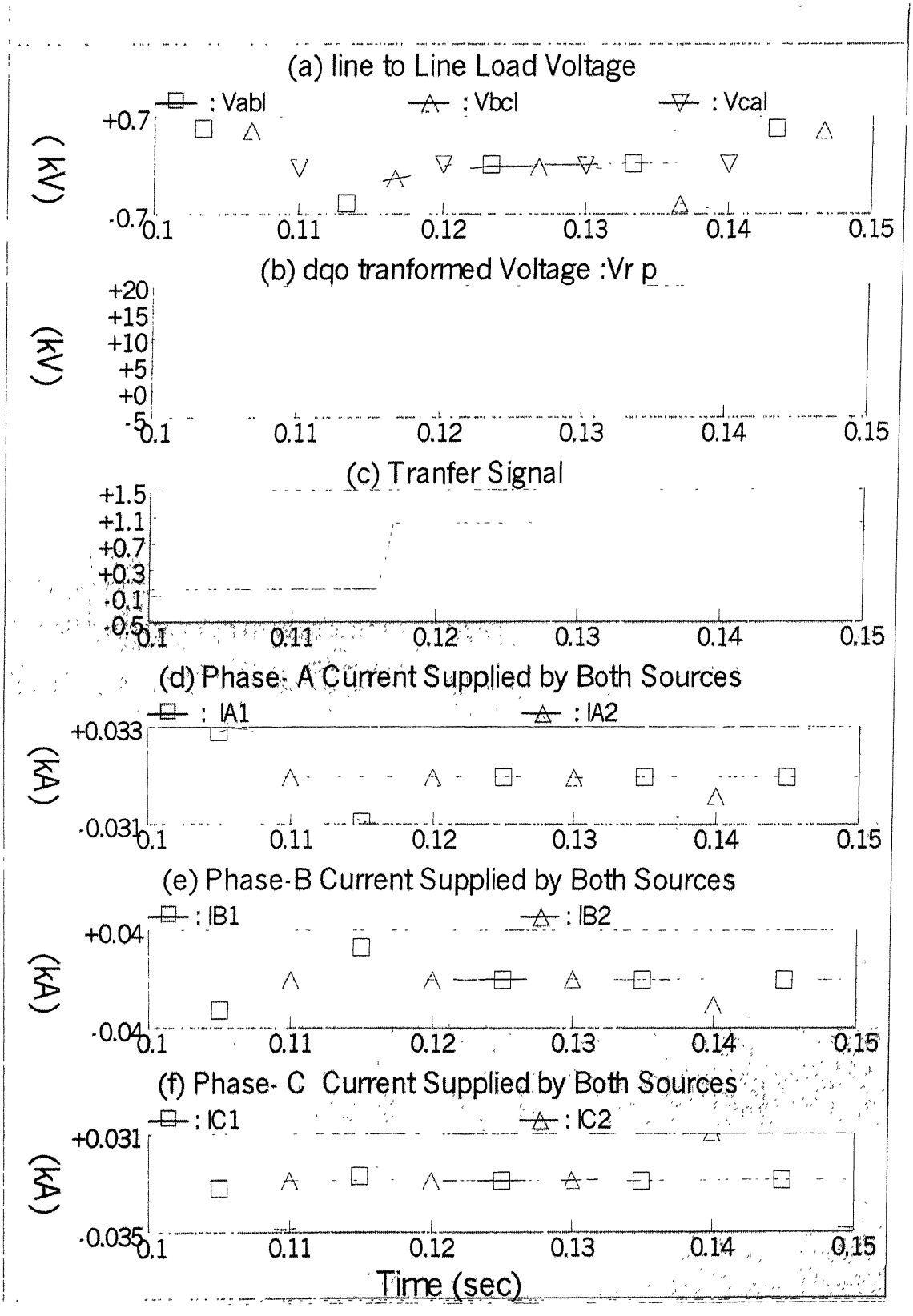

Fig. 4.6 R-L load, two phase to ground fault, system response

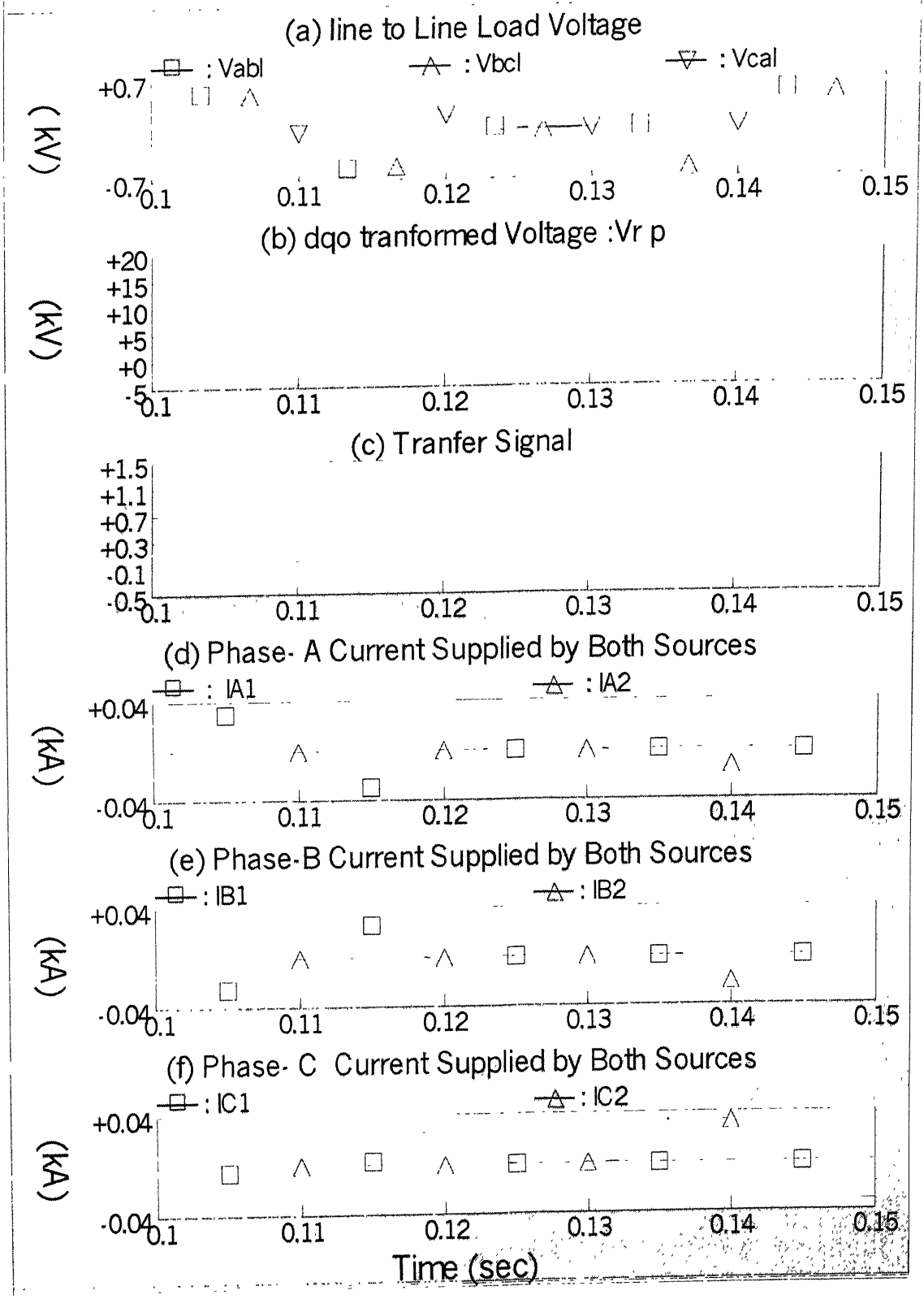

Fig. 4.7 R-L load, single phase to ground fault, system response

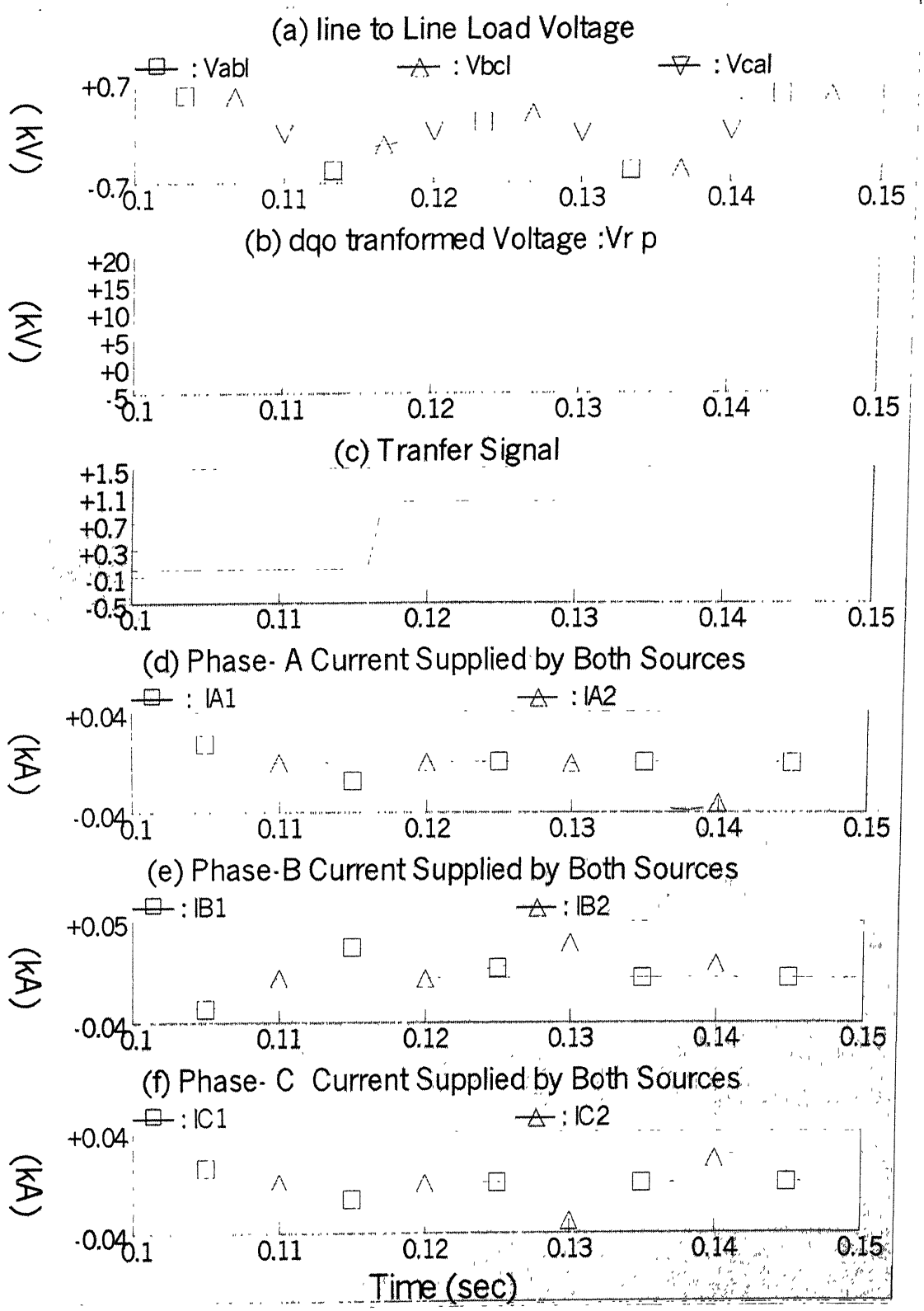

Fig. 4.8 Motor load, two-phase to ground fault, system response

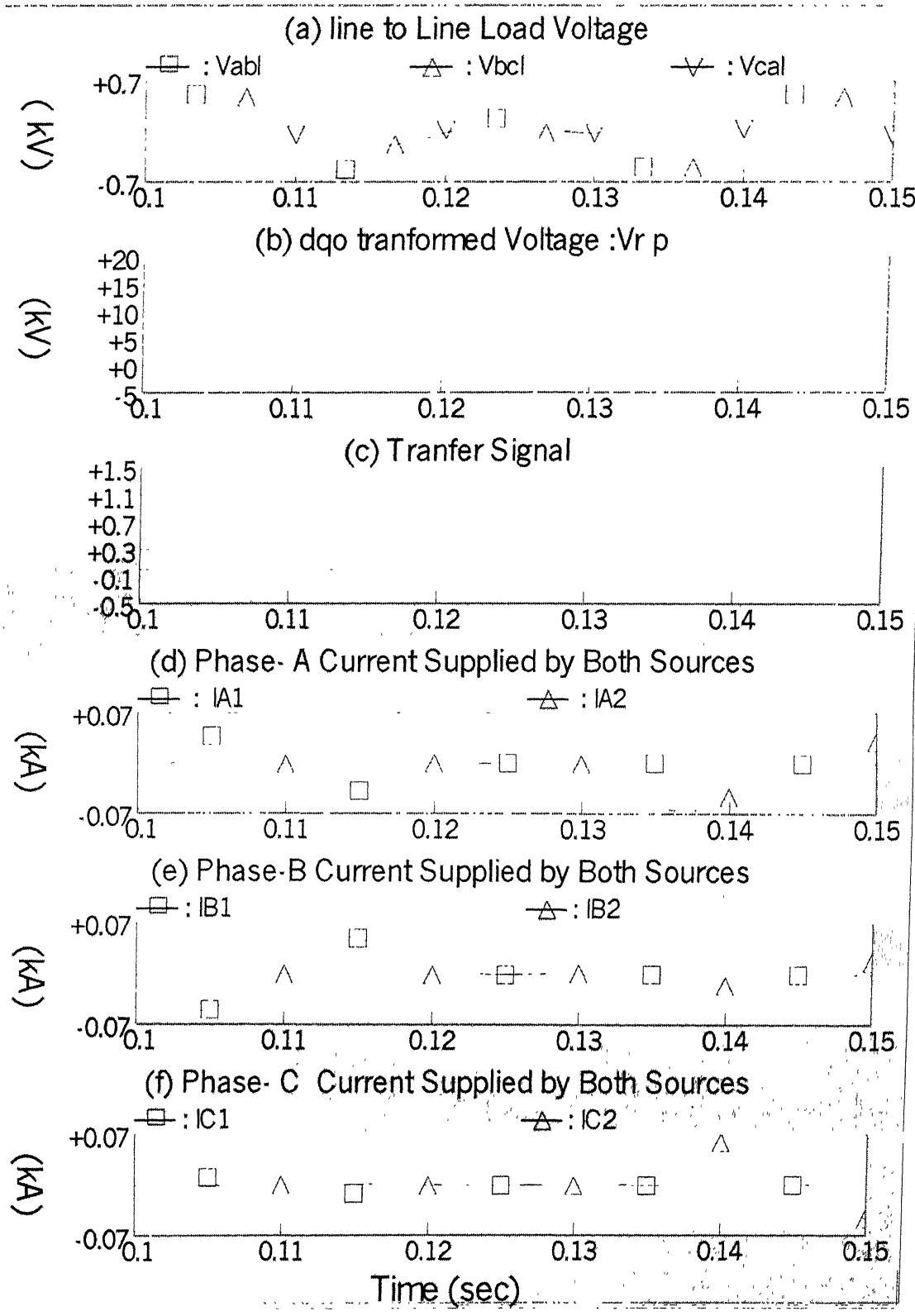

Fig. 4.9 R-L and motor load, two phase to ground fault, system response

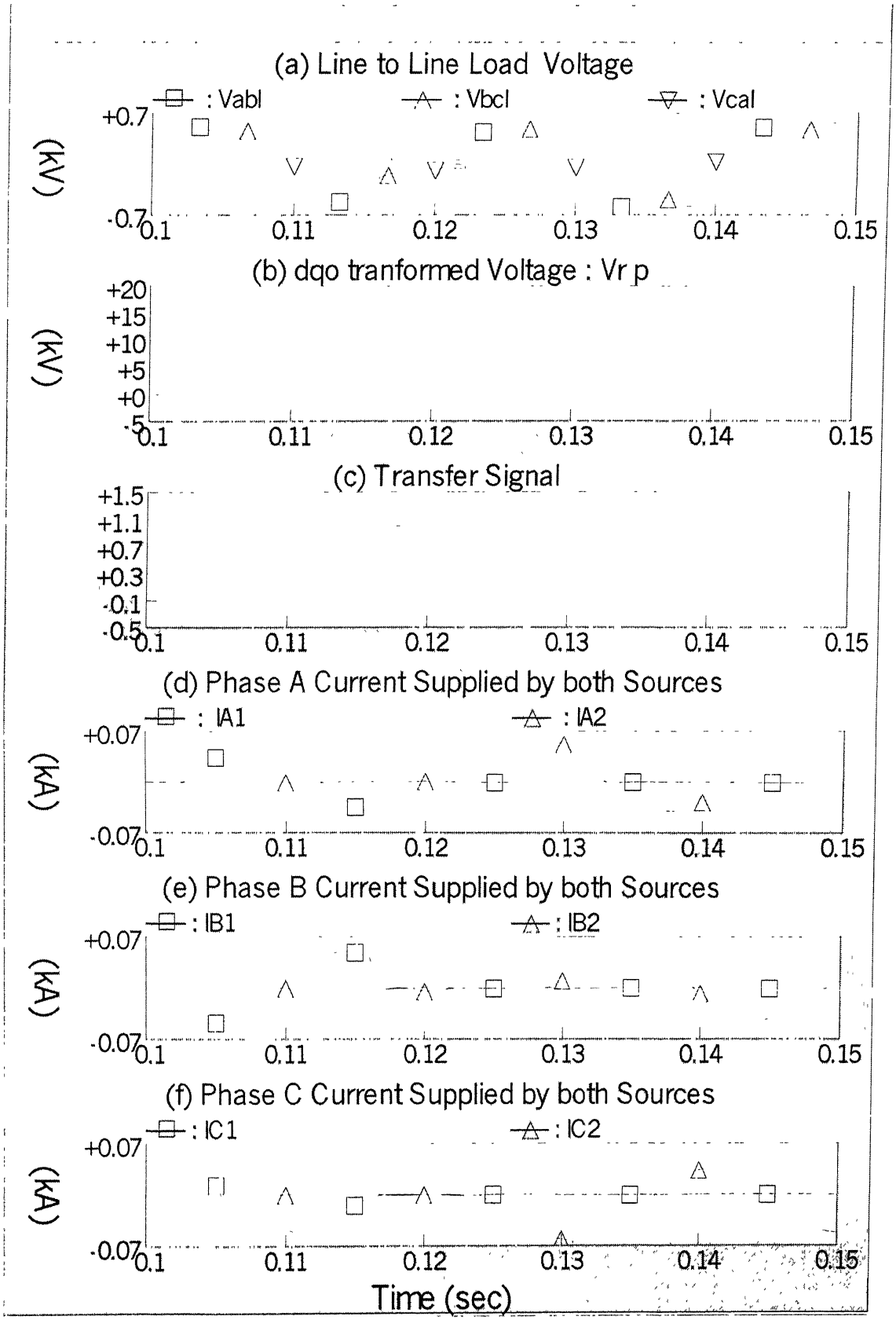

Fig. 4.10 R-L and motor load, two phase to ground fault, GTO based STS system

The simulation for combination of RL and Motor load is also performed and result is presented in Fig.4.9. Here regenerative does not affect the transfer process as it does feed the fault.

4.3.2 GTO based STS

The GTO based STS is simulated for the same R-L and motor load combination. The current is forced to zero instantaneously. There is no problem of cross current, thus current direction detection logic is not needed. Even regenerative load can not affect the performance of the STS. The transfer time observed for this is 6 ms second and this is almost constant for all the operating conditions. Total transfer time varies between 7 to 8 ms. This improves the power quality to a small extent. The drawback observed is that the transients appear at the time of transfer due to a finite current chopping by the GTO switches. But it does not affect much the sensitive load because they are present for less than 4 ms as shown in Fig.10.

4.4 Conclusions

The STS is an important device for improving the power quality for critical loads. PSCAD/EMTDC simulation is presented in this chapter for three-phase application of the STS. Simulation results for various fault conditions and load are compared. The detection time is a minimum for three-phase fault. The transfer time is dependent on type of load and it is higher for a regenerative load as compared to a passive load. The fault instant and the power factor of the load also affect it. The cross current phenomenon is also discussed which causes delay in load transfer and deteriorates the power quality. The GTO based three-phase STS is also discussed which transfer the load faster than SCR based STS.

CHAPTER 5

Conclusions

In this thesis various aspects of FRIENDS Devices and their Coordination issues have been studied. Power quality issues are currently receiving a great deal of attention in the light of distribution generation, deregulation, liberalization and privatization of the electrical energy market. There is important role of power electronics technologies in the future power delivery system The GTO based Static Current Limiter and Static Circuit Breaker topologies are currently in use. The SCR and GTO based Static Transfer Switch topologies have been used for protecting sensitive loads from voltage sag/swell. The SCL and STS are normally on devices while SCB is a normally off device. Thus SCB does not require the cooling system.

In this thesis, the SCL and SCB are simulated for an 11 kV radial distribution system. For simulation with SCL arrester clipping voltage levels of 6.9 kV and 13.8 kV are compared. It has been shown that the fault current transfers from static switch to let-through inductor and arrester within 4 ms. It is noted that increasing the arrester clipping voltage level reduces the arrester current and increases the current through let-thorough inductor. This will increase the voltage across the static switch, thus overvoltage protection becomes a considerable issue.

In case of SCB, the fault current is first transferred from VCB to static switch and it is then interrupted. The total interrupting time is 4 ms. The interrupting time for SCL and SCB is very small compared to their mechanically operated counterparts.

Coordination issues for protection FRIENDS Devices are simulated for a 11 kV generic distribution system. The protective devices must switch off the smallest portion of the network without affecting the majority of loads. This objective is accomplished through primary and back up protection using SCLs and SCBs. The results for possible fault locations are presented. Thus locations for SCLs and SCBs and their primary and secondary protection strategy is proposed.

The single-phase STS is simulated for both SCR and GTO based topologies and results are compared. The control strategies to transfer a sensitive load from preferred to alternative source in case of voltage disturbances are explained. The three-phase STS is simulated for passive R-L and regenerative loads. Cross current phenomenon is observed. The fault detection time is function of types of fault. This is maximum for single line to ground fault and minimum for three-phase to ground fault. The transfer time is dependent on type of load and it is higher for a regenerative load as compared to a passive R-L load but this is almost constant for GTO based topology.

The main contributions of the FRIENDS Devices for improving the power quality can be summarized as follows:

- Protection against power outages
- Mitigation of voltage sags and swells
- Power supply of different reliability
- Interface to dispersed generation systems
- Flexibility in Configuration of the System
- Load Leveling and Energy Conservation.

5.1 Scope for the future work

Some suggestions for future work are:

1. FRIENDS Devices are to be studied with existing power delivery system which is protected by mechanically operated devices.
2. Digital Signal Processing to control FRIENDS Devices is to be investigated.
3. Lumped feeder parameters are considered in this thesis, study with distributed parameters can be done.
4. Instead of individual semiconductor devices low loss modules are to be studied to reduce the conduction losses.
5. Experimental set up for validation of the simulation results is to be developed.

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APPENDIX A

Devices Specifications

SCR and GTO

Thyristor ON Resistance = 0.01 Ω

Thyristor OFF Resistance = 1.0E6 Ω

Forward Break over Voltage = 1.0E5 kV

Reverse withstand Voltage = 1.0E5 kV

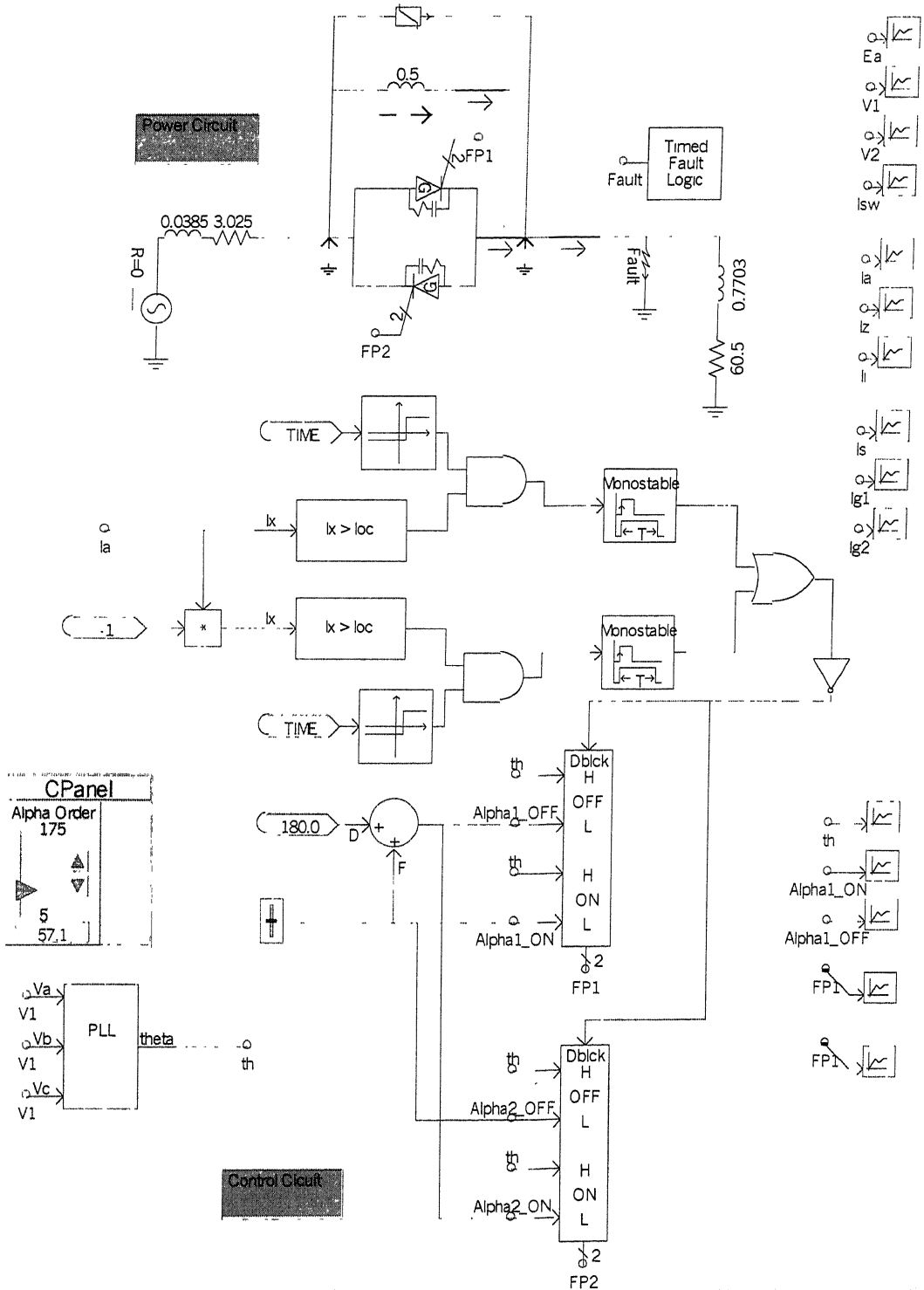
Snubber Resistance = 5 kΩ

Snubber Capacitance = 0.05 μF

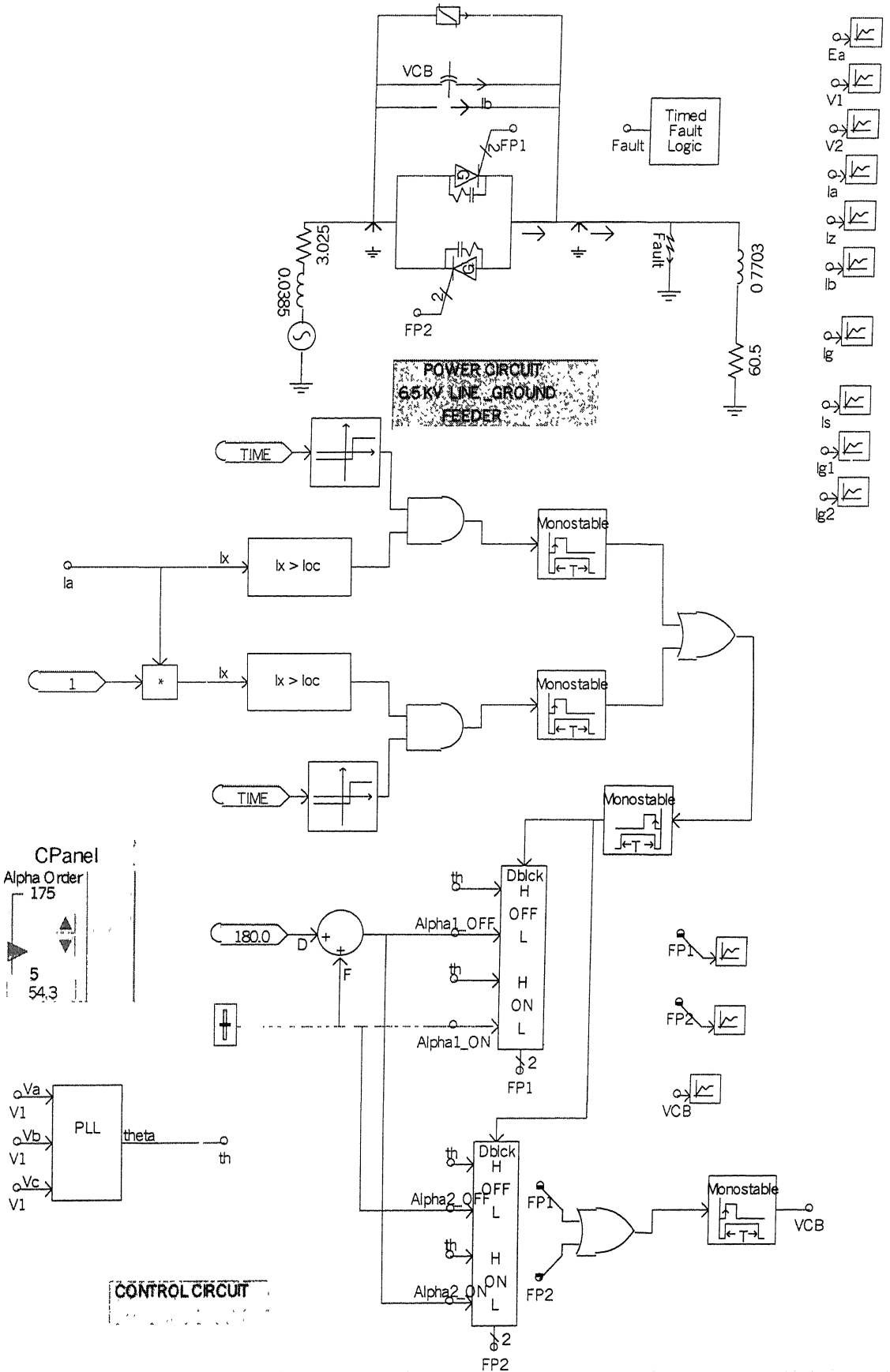
APPENDIX B

PSCAD/EMTDC Simulation Drafts

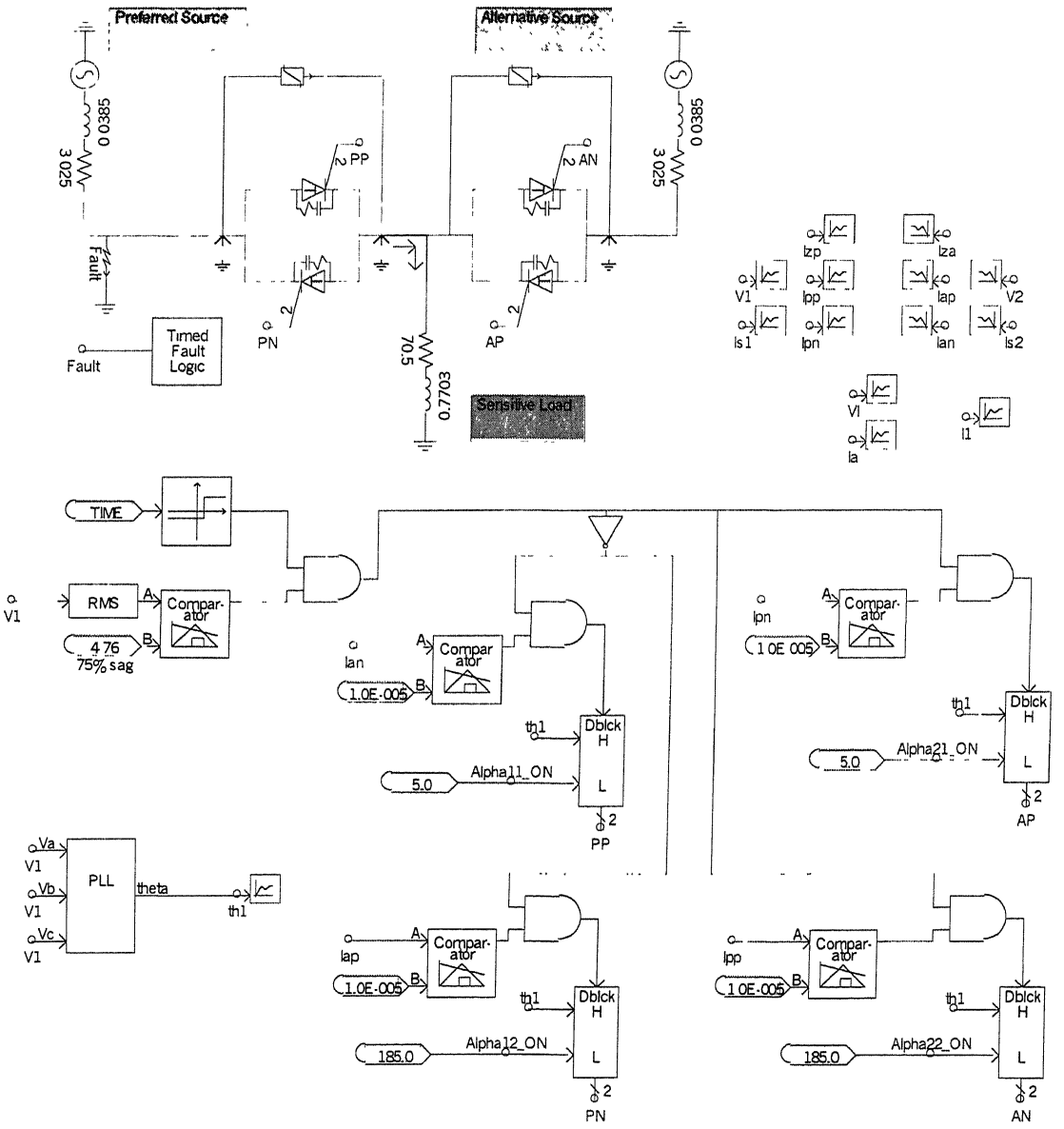
B.1 Static Current Limiter



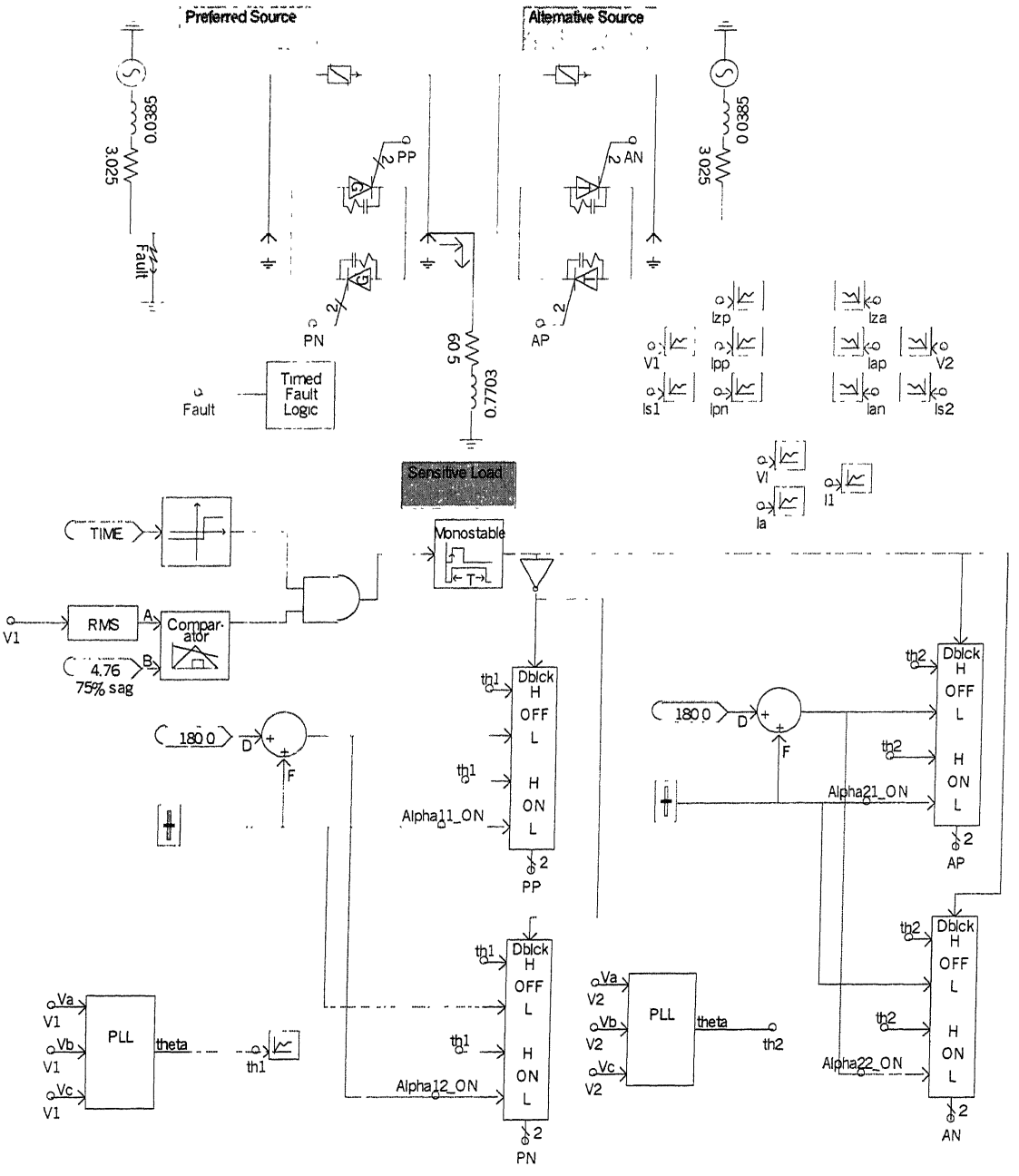
B.2 Static Circuit Breaker



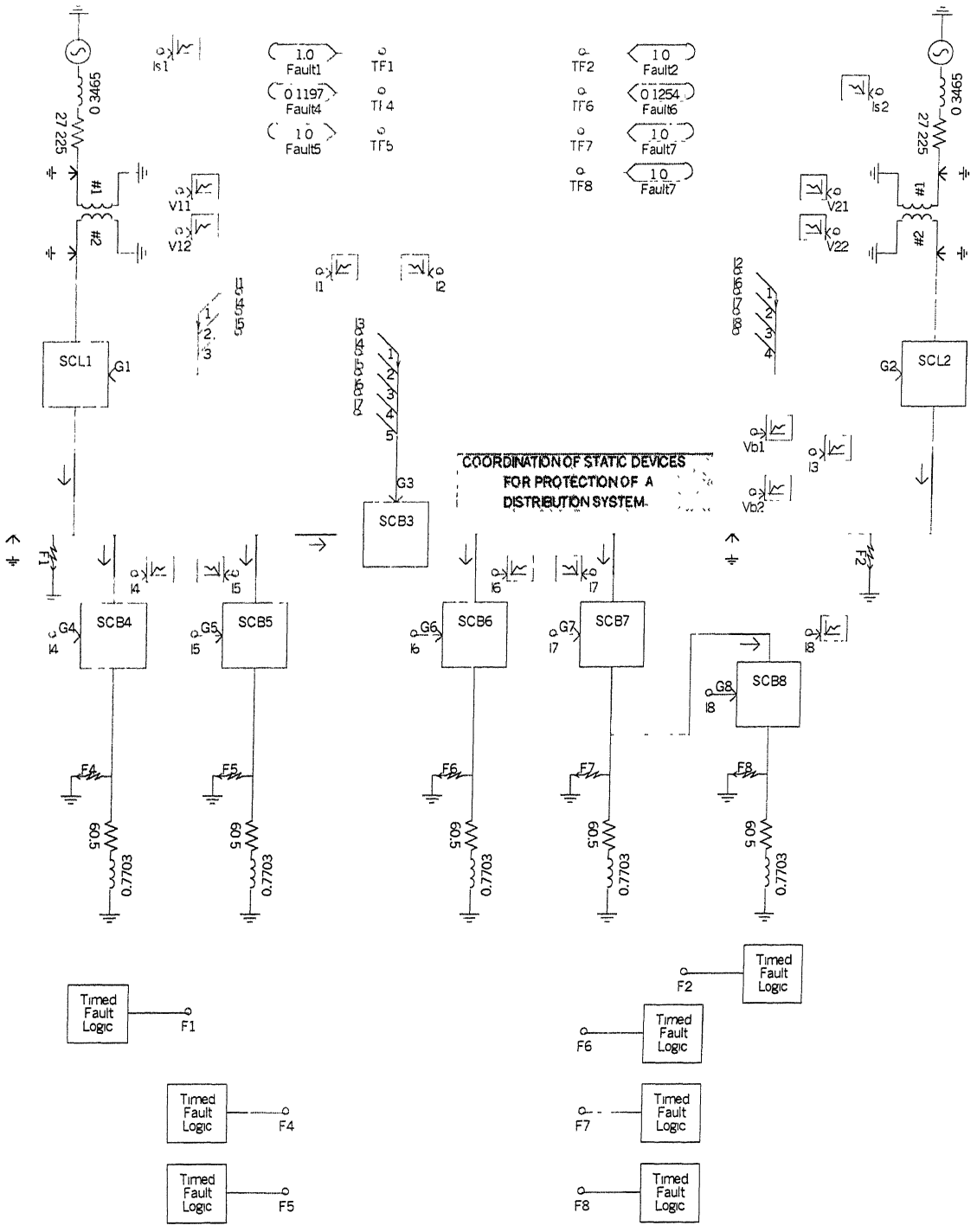
B.3 SCR Based Single Phase-Static Transfer Switch



B.4 GTO Based Single Phase-Static Transfer Switch



B.5 Coordination of FRIENDS Protection Devices



B.6 The Three-phase STS System